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Research Paper

Analysis of the Effect of Temperature and Power Dissipation Variations in SRAM Cells

Engineering

KEYWORDS : SRAM, Power Dissipation, Temperature, XNOR, Low Power memories.

V.Saminathan — Assistant Professor, Department of ECE, Maharaja Engineering College, Avinashi, India-641654

Dr.K.Paramasivam — Professor, Department of ECE, K.S.R College of Engineering, Tiruchencode, India-638401

ABSTRACT

With the increment of mobile, biomedical and space applications, digital systems with low-power consumption are required. As a main part in digital systems, low-power memories are especially desired. Reducing the power supply voltages to sub-threshold region is one of the effective approaches for ultra-low-power applications. The on-chip caches can reduce the speed gap between the processor and main memory. These on-chip caches are usually implemented using SRAM cells. In SRAM cell stand by leakage power has become a major issue in modern low power fabrication with technology scaling and for high temperature operations. Our paper has emphasized on power dissipation variations in 6T, 9T and ST10T SRAM cells. Here the effect of power dissipations is observed on various temperatures at different supply voltages. It is observed that in our proposed system the power dissipation goes from 0.007mw to 0.019mw for 27^{0}C to 127^{0}C respectively and it is less compared to 6T, 9T and ST10T SRAM Cells.

I. Introduction

Silicon memories have grown in size, density and speed over the last decade. This trend has been largely made possible by the ever shrinking dimensions of the MOSFET, which follows the so-called Moore's law where transistor count doubles every 18 months .However; memory scaling is losing pace with silicon scaling due to increasing device variation[1].To continue memory scaling, new memory circuits that can tolerate increased silicon variation are needed. SRAM is a volatile memory that uses two back-to-back logic inverters to store data. Fasts read and write data access can be achieved as the data is stored by active circuits. As a result of their fast access time, SRAM memories are utilized as a first level of storage for high speed processors, and as a memory of choice for system-on-a-chip implementations. However, process variation, specifically silicon variation, is preventing further increase to SRAM density as key transistor parameters are becoming ever more random[2][3].

II. 6T SRAM CELL

A 6T bit cell comprises of two cross-coupled CMOS inverters, the contents of which can be accessed by two NMOS access transistors. The 6T bit cell is the default memory bit cell used in the present SRAM designs. A single-ended 6T bit cell uses a full transmission gate at one side. Write-ability is achieved by modulating the virtual VCC and virtual-VSS of one of the inverters. It consists of two cross-coupled inverters and two access transistors. When the horizontally-running word-line is enabled, the access transistors are turned on, and connect the storage nodes to the vertically-running bit-lines. In other words, they allow access to the cell for read and write operations, acting as bidirectional transmission gates.

Table I
Modes of SRAM

MODES	WL	WWL
Read mode	0	1
Write mode	1	1
Hold mode	0	0

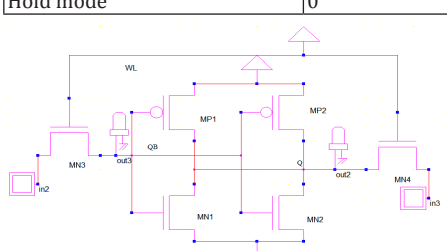

Fig.1 6T SRAM Cell

A. Working of 9T SRAM cell

In 9T-SRAM cell to save the power during write operation, a tail NMOS transistor N7 is connected in the pull-down path of one of the inverter. Our proposed circuit is similar to ZA cell with some Difference. Gate of tail transistor N7 is connected to bit line BL instead of extra signal WS as in case of ZA cell .This arrangement saves area on the chip as well as timing conflict in between WS and write-word line. An extra NMOS transistor N6 is connected in between two inverters so that during read operation cell behaves as conventional 6T SRAM cell.

Switching activity of this transistor is controlled by read word line. Due to transistor N6, effective resistance of the pull down path of inverter is reduced compared to ZA cell and results in lower read power consumption. Read operation is performed through access transistor N5 and RBL bar.

B.Working of ST10T SRAM cell

The operating principle of our 10T SRAM can be summarized as follows using the timing diagram. In read mode, WL is enabled and VGND is forced to 0 V while remains disabled. The disabled makes data nodes decoupled from bit line during the read access. Due to this isolation, the read SNM of our 10T cell is almost same as the hold SNM of conventional 6T cell. Since hold SNM is much larger than read SNM in the 6T cell, read stability is remarkably improved in our 10T cell. Depending on the cell data value, one of the bit lines starts discharging after WL is enabled.

III. Proposed System

Today, even as many aspects of CMOS dev\ice scaling begin to saturate off the exponential trend, density scaling remains a primary objective of the semiconductor industry. In the face of rapidly emerging limitations that are fundamental to continued device shrinking, density-scaling enables circuit and architecture level parallelism, providing a means to achieve energy-efficiency and performance improvements in lieu of the previous trend.

Embedded SRAMs provide a direct means of bringing the benefits of transistor level density-scaling to the circuit and architecture levels and are therefore vital to this new model of IC scaling. Due to their regular structure and broad applicability to so many digital systems, SRAMs are carefully designed as one of the lead components during the development of new technology nodes, and they utilize highly specialized and aggressive layout rules that address sub-resolution fabrication limitations.

This level of design attention has allowed SRAM bit-cells to follow density trends in-line with the transistors themselves. Embedded SRAMs are a critical component in modern digital systems, and their role is preferentially increasing. As a result, SRAMs strongly impact the overall power, performance, and

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area, and, in order to manage these severely constrained trade-offs, they must be specially designed for target applications. MOSFET designs and their benefits for extending density and voltage scaling of static memory arrays.

The proposed work is to analysis the power dissipation variations in 10T SRAM cell [4]. This technique uses a concept of scaling to reduce the area. The proposed system makes use of an XNOR gate and the tail transistor in an array that is shared by all the cells in a row to reduce the area overhead. Therefore, as the word-size increases, the area overhead per cell reduces.

The use of column- and row-wise techniques amounts to only a small, yet significant, reduction in SRAM cell area under increasing Vt variation. On the other hand, novel SRAM cell topologies, that utilize more than the standard six transistors, are capable of providing more robust read and write operations in the presence of Vt variation, but at the cost of initial area overhead.

The circuit diagram and layout of the proposed 10T SRAM cell are shown below

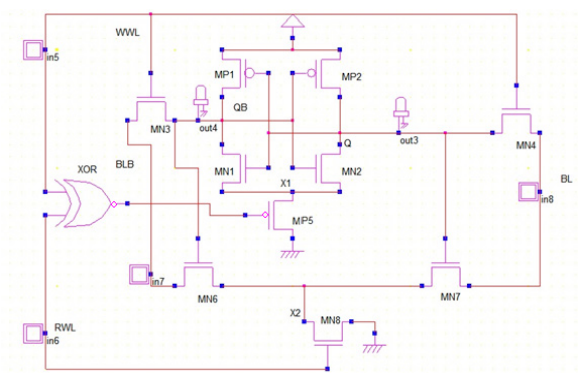

Fig.2 Proposed 10T SRAM Cell

The reduced t_{ox} causes gate leakage due to various leakage mechanisms such as Fowler–Nordheim tunnelling, direct tunnelling, hot-carrier injection, etc.Due to high drain voltage and negative gate voltage, field crowding occurs at the drain edge, resulting in gate-induced drain leakage. When a high drain voltage is applied to a short-channel de-vice, the barrier height is lowered and the point of the maximum barrier is shifted toward the source end, resulting in drain-induced barrier lowering and decrease in V_t. At even shorter channel lengths, the drain end depletion layer extends and may touch the source end depletion layer, resulting in a punch through condition.

A. Operation

The critical design strategy of SRAM cell is the series connection of a tail transistor. The gate electrode of this device is controlled by the output of an XNOR gate, inputs of which are tapped from write word line and read word line control signals coming from the WWL and the RWL drivers. The XNOR gate and the tail transistor are shared by all the cells in a row. The tail transistor has to be appropriately up-sized for sinking currents from all the cells in the row.

However, a minimum sized tail transistor is used .The read buffer of the cell is designed with up-sized devices to achieve shorter read delay and higher read stability. Without this read buffer, a cell with such small drivers and series-connected tail transistor would exhibit unacceptably low read static noise margin, resulting in read instability.

B.Read Operation

In case of 6T, BLs are precharged, MN1 is ON, storage node "L" stores a "0," and "H" stores a "1". When WL is activated, BLB drops through MN3/MN1.In 10T, "L" and H" are isolated by deactivating WWL, "0" in "L" turns MN6 OFF, and "1" in "H" turns MN7 ON, which raises the internal node voltage to a value higher than zero. When RWL is activated, raised X2 offers body effect to MN7. Due to positive VX2, body-to-source voltage Vbs, MN7 becomes negative, resulting in an increase in the threshold voltage of MN7.

This results in reduction in its drive strength. Hence, it takes longer time to discharge BL. This is not the case with a 6T cell. In a 6T cell, node "L" initially remains at ground level and gradually increases to a higher value due to the voltage dividing effect. Therefore, body effect in MN3 is comparatively much smaller. Moreover, CBL/CBLB of LP10T is double compared with that of 6T. Therefore, it requires longer time to reach read point. Our bit cell exhibits narrower spread in read delay at all considered VDD.

C. Write Operation

For writing "0" to storage node "L" from the time when WWL is activated to the time when "L" falls to 10% of its initial high level. Similarly, for writing "1" to "L" is estimated from the time when WWL is activated to the time when "L" rises to 90% of its full swing from its initial low level. This avoids miswrite.

D. Stacking Effect

The leakage in our cell can be reduced by using the stacking effect. In a two-device stack, if the upper device connected to VDD is ON and the bottom device is OFF, the internal node voltage is raised to a value higher than zero. In hold mode, the tail transistor is turned OFF by the low output of the XNOR gate, since both of its inputs remain low in hold mode. This breaks the ground path of the cross coupled inverters. As the bottom transistor is OFF in a two-transistor stack formed with MN1 and MP3, in this particular case, when H holds "1," the internal node X1 is raised.

The positive VX1 offers a stacking effect that helps in reducing standby power during hold mode. The internal node X2 is also raised in hold mode due to the stack formed with MN7 and MN8. This causes negative VGS, negative VBS, and reduced VDS in top devices. The sub-threshold leakage is the major component that is reduced due to stacking effect.

E. Low Voltage Operation

During a write operation the power supply to the side of the cell being pulled low is turned off in the 10T cell, which allows the external write drivers to pull the logic-1 node easily below the trip point of the back-to-back inverters. In the case of the 6T cell, the external write drivers must fight against an active PMOS device, which keeps the logic-1 node high until the cell starts to flip. Vt variation of this minimum sized PMOS device causes variation in the time required to successfully pull a logic-1 storage node low, and in some cases results in the inability to pull this node low enough to cause the cell to flip.

IV. Simulation Results

The simulation for different voltages was carried out and corresponding response time was observed. The analysis shows that there is a significant reduction in terms of power dissipation .The SRAM cells also exhibit different power variations depending on the temperature .The simulated waveforms taken for voltage Vs time for 6T,9T,ST10T,10T SRAM cells are shown below

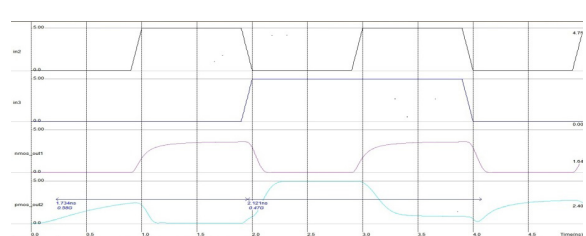

Fig.3 Voltage Vs Time Waveform for 6T Cell

The above Fig.3 shows the voltage Vs time waveform for 6T SRAM cell. Here for the in2 the voltage remains low up to 1ns and remains high for the next 1ns.For the in3 the voltage remains low up to 2ns and remains high for the next 2ns. The voltage at the NMOS out1 remains 0 up to 1ns and goes to some

value for the next 1ns time period.

Fig.4 Voltage Vs Power Curve For 10T Cell

The above Fig.4 shows the variation of leakage power dissipation in mw with respect to the various supply voltages .Here 10T shows power dissipation of 0.248mW for 2.0V supply and it shows power dissipation of 0.513mW for 5V supply. 10T shows less power dissipation when compared to 6T and ST10T.

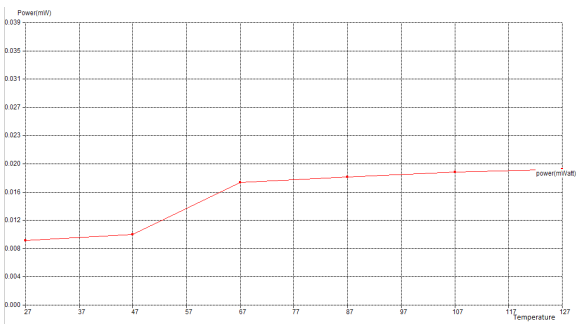

Fig.5 Temperature Vs Power Curve for 10T Cell

The above Fig.5 shows the variation of leakage power dissipation in mw with respect to the various temperatures in 10T. From this it's clear that the power dissipation in 10T is less than 6T, 9T and ST10T

A. Comparison Result

The performance metrices of the SRAM cell can be determined by comparing the power dissipation with respect to the supply voltage. Here the 10T SRAM cell shows less power dissipation for 2mV and 5mV power supplies and for various temperatures compared to 6T, 9T and ST10T SRAM cells as shown in Table II and Table III respectively.

Table II
Comparison Result for Temperature Vs Power Dissipation

Temperature	6T	9T	ST10T	10T
27	0.327	0.209	0.098	0.007
47	0.345	0.224	0.145	0.010
67	0.356	0.265	0.178	0.017
87	0.398	0.288	0.216	0.018
107	0.442	0.3	0.248	0.018
127	0.461	0.315	0.265	0.019

Table III
Comparison Result for Voltage Vs Power Dissipation

SRAM CELL	V_{DD} (mV)	POWER DISSIPATION (mWatt)
6T	2.0	0.622
	5.0	3.571
9T	2.0	0.322
	5.0	2.872
ST10T	2.0	0.270
	5.0	1.533
LP10T	2.0	0.092
	5.0	0.216

V. CONCLUSION

This paper presented a analysis the effect of power dissipation variations at various temperatures and supply voltage V_{DD}. The proposed 10T cell is compared with traditional 6T, 9T and ST10T SRAM cell on MICROWIND simulator for 60nm at wide range of supply voltage and temperature. It is observed that in our proposed system the power dissipation goes from 0.007mW to 0.019mW for 27^0C to 127^0C respectively and it is less compared to 6T, 9T and ST10T SRAM Cells.

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