Volume : 2 | Issue : 12 | December 2013 • ISSN No 2277 - 8179

Research Paper

Metaheuristic Approach for VLSI 3D-Floorplanning

Engineering

KEYWORDS : 3D VLSI Technology, Floorplanning, Metaheuristic Technology, Simulated Annealing

Mr. Lalin L. Laudis — M.Tech Student, Dpartment of Electronics and Communication Engineering, Vel Tech Dr.RR.& Dr.SR Technical university, Chennai.

Mr. Amit Kumar Sinha — Assistant Professor, Department of Electronics and Communication Engineering, Vel Tech Dr.RR.& Dr.SR Technical university, Chennai

ABSTRACT

From the period of evolution of VLSI began; floor planning for the physical design was the most important problem to concern about. Modern three-dimensional (3D) chips are based on the fact that, the active devices are placed in multiple layer using 3D integration technologies. Though the 3D chips are latest, the growth and progress in the development are not up to the mark. The complex problem to be viewed in 3D VLSI design is the floorplanning part. The two Dimensional VLSI chips which are in application today also encountered the same floorplanning problem. In three dimensional VLSI chips, as the devices are placed in multiple layer, the placement of blocks play a vital role in the chip size. It seems to be a herculean task for the designers for placing the components in the proper place with efficient usage of available place. In this paper a solution to the modern 3D VLSI floor planning is proposed based on a a algorithm named simulated annealing. It is expected that the algorithm would work more efficiently in 3D VLSI chips as the same algorithm produced more optimal solutions for various benchmark problems in 2D VLSI floorplanning.

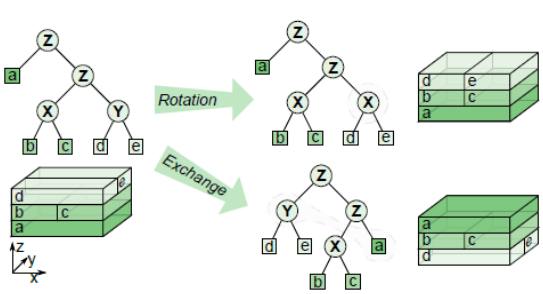
Introduction

VLSI has earned a lots of scope in this era. The fast growing world need everything to be optimized and henceforth, very large scale integration is an interesting area to be concentrated by researchers. Though, the field has lots of development, the progress is not up to the mark. This is because of several constraints and limitations in the field. Today in practice, Two Dimensional (2D) chips are in practice. Yet, the problems associated with are also increasing day by day. Hence research focus on VLSI floorplanning is also greatly increasing. Inspite of all these problems, the new technology named Three Dimensional (3D) also has been proposed. As a dimension has increased the problem of floor planning has also increased. This research work propose a metaheuristic algorithm named, Simulated Annealing (SA) [4] for solving the floorplanning problem in 3D VLSI floorplanning.

3D- VLSI Floorplanning

In VLSI 3D floorplanning, the devices are placed in multiple layers which is a promising option for keeping the Moore's law into effect. Also 3D designs are only slowly gaining practical importance as the design faces lot of technical and physical design problems. In general, the geometric representation of the various components are assigned a location and followed by routing process and then simulated and optimized. In the physical design of the 3D circuits, various parameters viz, heat dissipation must be considered. In conventional 2D circuits, a wide variety of algorithms were used to optimize the floorplanning problem. Several data structures were also used to place the blocks in the proper place. In 3D planning, the same data structures [6] are used like 3D slicing tree as shown in figure. Yet, this is limited to slicing floorplans alone[5].

Fig 1 : 3D Slicing opration.



The general floorplanning problem can be stated as follows: Let B ¼ {b_1, b_2, . . . , b_m} be a set of m rectangular modules whose respective width, height, and area are denoted by wi, hi, and ai, 1 ≤ i ≤ m ,Each module is free to rotate. Let (x_i, y_i) denote the coordinate of the bottom-left corner of module bi, 1 ≤ i ≤ m, on a chip. A floorplan F is an assignment of (x_i, y_i) for each bi, 1 ≤ i ≤ m, such that no two modules overlap with each other. The goal of floorplanning is to optimize a predefined cost metric such as a combination of the area (i.e., the minimum bounding rectangle of F) and wirelength (i.e., the sum of all interconnection lengths) induced by a floorplan. For modern floorplan designs, other costs such as routability, power, and thermal might also need to be considered. We can classify floorplans into two categories for discussions: (1) slicing floorplans and (2) non-slicing floorplans. A slicing floorplan can be obtained by repetitively cutting the floorplan horizontally or vertically, whereas a non-slicing floorplan cannot. A floorplan is sliceable if its rectangular dissection can be obtained by recursively dividing rectangles into smaller rectangles until each non-overlapping rectangle is invisible. All floorplans may not be sliceable, and such plans are called non sliceable floorplans Sliceable floorplans are represented by a binary tree whose leaf nodes denote modules and internal nodes denote horizontal or vertical cut lines. As this representation cannot be used for non slicing floorplans of VLSI circuits, researchers have devised representations for non slicing floor plans such as Sequence Pair (SP) , Boundary Slicing Grid (BSG) , Otree, B*tree and others The pictorial representation of slicing and non slicing operation if given in the following figure 2.

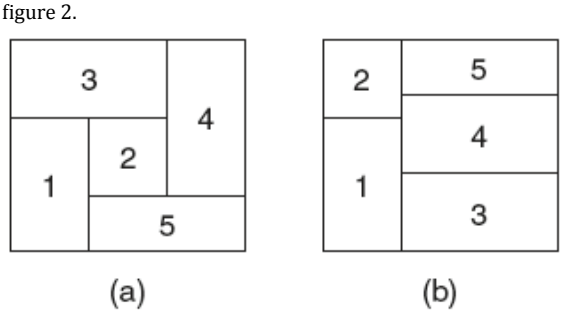


Fig 2 : (a) non- slicing floor planning ; (b) Slicing floor planning

A 3D circuit is the stack over outcome of regular 2D circuits. The advances on the fabrication and packaging technologies allowed interconnecting stacked 2Dcircuits by using 3D vias. However, 3D-vias can impose significant obstacles and constraints to the 3D placement problem. Most of the existing placement al-

gorithms completely ignore this fact, but they do optimize the number of vias.

Vlsi floor planning problem described must be optimized somehow. The role of algorithms come in to picture at this position. It is a difficult task for human to find the optimal solution and hence it is done by using some algorithms. The role of an algorithm is to find a more optimal solution which satisfies the given constrains and converge to its best. Several algorithm viz, Generic algorithms (GA), Evolutionary algorithms (EA)[7] were proposed during last century. But every algorithm has a advantage over other one and in the same way it has some cons. also over others. On studying in depth about the various algorithms used for optimization, Simulated annealing (SA) was found to be the best for floor planning problems. The previous works made be researchers prove that multi objective optimization using simulated annealing (AMOSA) [8] gave a more faithful results that any other algorithms.

simulated annealing

Simulated annealing is a technique introduced in 1982 by Krkpatrick , with an unusual pedigree: it is motivated by an analogy to the statistical mechanics of annealing in solids. To understand why such a physics problem is of interest, consider how to coerce a solid into a low energy state. A low energy state usually means a highly ordered state, such as a crystal lattice; a relevant example here is the need to grow silicon in the form of highly ordered, defect-free crystals for use in semiconductor manufacturing. To accomplish this, the material is annealed i.e, heated to a temperature that permits many atomic rearrangements, then cooled carefully, slowly, until the material freezes into a good crystal. Simulated annealing techniques use an analogous set of "controlled cooling" operations for nonphysical optimization problems, in effect transforming a poor, unordered solution into a highly optimized, desirable solution. Thus, simulated annealing offers an appealing physical analogy for the solution of optimization problems, and more importantly, the potential to reshape mathematical insights from the domain of physics into insights for real optimization problems.

Simulated Annealing Algorithm has been proved to be very simple compared to GA and PSO methodologies and widely used for floorplanning. It is an optimization scheme with non-zero probability for accepting inferior (uphill) solutions. The probability depends on the difference of the solution quality and the temperature. The probability is typically defined by;

$$\text{Probability} = \min\left\{1, e^{(-\frac{\Delta c}{T})}\right\}$$

where Δc is the difference between the cost of the neighboring state and current state, and T is the current temperature. In the classical annealing schedule, the temperature is reduced by a fixed ratio λ, for each iteration of the annealing process. Another dimension of simulated annealing is fast simulated annealing (FSA) Fast Simulated Annealing processis to integrate the random search with hill climbing more efficiently. Unlike the classical SA, the annealing process consists of three stages: (1) The high-temperature random search stage, (2) the pseudogreedy local search stage, and (3) the hill-climbing search stage.

proposed methodology

In this paper, it is proposed that the most effective algorithm for finding optimal solution i.e simulated annealing can be applied to solve the floorplanning in 3D VLSI chips. The work can be tested under several dimensions of simulated annealing i.e, Fast Simulated Annealing (FSA)[1], spheroidizing Simulated Annealing (SSA) [4]. The algorithm produced more convergence rate when compared to conventional algorithms. Henceforth, the placement of components in a perfect place and to use the available place in an optimal manner is achieved. The conclusion was made as the simulated annealing algorithm proved itself with more accuracy in finding the best solution and the convergence rate was much higher. The proposed algorithm may be checked with some of the test problems and the convergence rate may be measured. Thus the algorithm has a much scope in solving the VLSI floorplannig in 3D. The pseudo code for simulated annealing algorithm is given below.

Fig 3. Simulated Annealing Algorithm- Pseudocode

```
s ← s0; e ← E(s)                    // Initial state, energy.
s_best ← s; e_best ← e              // Initial "best" solution
k ← 0                               // Energy evaluation count.
while k < k_max and e > e_max       // While time left & not good
                                    //enough:
T ← temperature(k/k_max)            // Temperature calculation.
s_new ← neighbour(s)                // Pick some neighbour.
e_new ← E(s_new)                    // Compute its energy.
if P(e, en_ew, T) > random() then // Should we move to it?
s ← s_new; e ← e_new                // Yes, change state.
if e_new < e_best then              // Is this a new best?
```

CONCLUSION

The floorplanning problem in VLSI 3D chips are found to be NP hard and hence only by using some algorithms the perfect solution set is obtained. This proposed algorithm can be expanded using multi objective optimization (MOSA) and several other dimensions of simulated annealing viz, FFA,SFA etcetera. The authors are working towards the direction of conducting brief analytical and theoretical study of SA and its convergence rate in optimizing a multi objective optimization problem (MOO) and hence the usage of SA and its derivative could be used for modern 3D VLSI chips and to make the chips more smarter and compact..

Acknowledgment

The authors would like to thank Dr.S.Anand, Assistant Professor, V.V.College of Engineering for his strong motivation and guidance in the publication of this paper.

REFERENCE

[1] Tung Chein Chen, Yao-Wen Chang "Floorplanning," Chapter 10, pp. 575–631. | [2] Nikhil Gupta "Genetic algorithm based partioning of VLSI circuit System" Natioinal conference on future aspects of artificial intelegence in industrial automation", 2012 by international journal of computer application, pp. 15–19.. | [3] Robert Fischbach, 3D Physical Design Challenges and solutions., Institute of Electromechanical andElectronic Design. | [4] S.Anand, "Customed simulated annealing based decision algorithms for combinatorial optimization in VLSI floorplanning problem". Springer , computational optimization an application , vol. 30 No. 2. Feb 2005. | [5] Jianli chen, "A hybrid simulated annealing algorithm for non slicing VLSI floorplanning" IEEE Trans.on system, man and cybernitics – part c., vol. no. 4,july 2011,pp 544-553., to be published. | [6] Tung – Chieh chen," mordern floorplanning based on B* tree and fast simulated annealing" IEEE Trans. Computer-Aided Design Of Integrated Circuits And Systems.,vol. 25, No. 4, April 2006 PP.637-650. | [7] Kripatrick, S., Gelatt, C., vecchi, M., : Optimization by Simulated Annealing Science 220(4598), 671–680 (1983) | [8] C. Coello, D. V. Veldhuizen, and G. Lamont, Evolutionary Algorithms | or Solving Multi-Objective Problems. Boston: Kluwer AcademicPublishers, 2002. |