Volume : 2 | Issue : 1 | Jan 2013 • ISSN No 2277 - 8179

Research Paper

Engineering

KEYWORDS :CMOS Technology, feedback network, low noise amplifier (LNA), peaking network, bandwidth extension.

A 17dB Gain LNA using 0.13µm CMOS Technology with Bridge-Shunt-Series Network

Mr. Hemantkumar. M. Vyas — M.Tech-VLSI student, Mewar University - Chittorgarh

P. R. Patel — Associate Prof. Electronics & Communication Ganapat University

ABSTRACT

The present paper contains the design of wideband LNA which combines a narrowband LNA topology with a resistive shunt feedback. The input matching for design has achieved by resistive shunt feedback furthermore reducing the Q-factor of the narrowband LNA input and rising the flattens of gain. Moreover design exhibit output peaking Bridged-Shunt-Series network to achieve bandwidth extension. The present LNA design has implemented in 0.13-µm CMOS technology to get 1-8GHz Ultra Wideband System. The present work has simulated with the software EDA tool T-SPICE and BSIMV3 model for 0.13-µm CMOS process. The present design of LNA gives Gain of magnitude 17dB and the noise spectral density of about -180dB with the total amount of power consumption of 6.2mW. Further the post layout of the design has carried out using MICROWIND Tool.

I. Introduction

Demand for low cost and high data-rate wireless communication systems is increasing. Since the FCC has authorized communication in the 3.1 GHz to 10.6 GHz frequency band, several technologies have been developed to satisfy the communication market. In integrated UWB systems the LNA must provide a high voltage gain on a high impedance output load given by a digitizer or a pulse detector in Impulse Radio UWB architectures. Further LNA is one of the most important block of the receiver. To achieve low cost design, LNA must be fully integrated and should consume low power and low die area. Ideally the LNA must be broadband matched to a 50Ω antenna, and must provide a high voltage gain on a high impedance value capacitive output load.

One of the major challenges in wideband communications systems is the design of a wideband low-noise amplifier (LNA). As the first active component in the receiver chain, LNA should offer appropriate and comparable gain such that giving a low noise to keep the overall receiver noise figure as possible as low. In addition, gain-flatness over the entire frequency range of interest is necessary to meet the design specifications. These properties are the cornerstones of the wideband LNA design which affect the total broadband communication system characteristics. Among wideband designs, distributed and common-gate amplifiers suffers from high noise figure. Additionally, cascading of several stages degrades the linearity of the LNA [5]-[6].

The present work contains design of Low Noise amplifier for WB communication system using 0.13-µm CMOS technology with source inductor degeneration and resistive feedback topology to achieve wideband input matching further bridge-shunt-series peaking network to achieve the wideband output response. In bridge-shunt-series peaking network, better bandwidth extension ratio (BWER) is achieved using capacitive splitting-an inductor is inserted to separate the total load capacitance into two constituent components [1].

II. Wideband Amplifier Design

A proposed Wideband LNA design can be achieved by using the resistive feedback topology with narrowband LNA design as shown in figure 1(a). This feedback amplifier consisting of a cascode transistor pair M_1 and M_2 as shown in figure 1(a). Capacitor C_F works as DC blocker to the gate of the M_1. The bias voltage V_{bias} provides DC bias for the input transistor M_1. The bias voltage V_{bias} can be generated by designing the voltage divider using CMOS [10]. The cascode transistor improves the isolation and reduces the Miller capacitance while the voltage gain of input transistor M_1 should be small. Inductor L_g performs series resonance with C_{gs} of M_1 for input impedance matching.

$$L_s = \frac{R_s}{\omega_t} \quad (1)$$

Where ωt = transition frequency of M1.

$$L_g = \frac{1}{(\omega_0^2 C_g)} - L_s \quad (2)$$

To broaden 3-dB bandwidth, the LNA employs the bridged-shunt-series peaking network as shown in figure 1(a) further to achieve wideband output matching source follower buffer can be designed. The value of Rf should be much larger than the conventional resistive shunt feedback. However, in the proposed topology input impedance is determined by ωT Ls. The important role of the Rf is to reduce the Q-factor of the circuit. The Q-factor of the circuit in figure 1(b) is given by

$$Q_w \approx \frac{1}{\left[R_s + \omega_t L_s + \frac{(\omega_0 L_g)^2}{R_{fn}}\right]\omega_0 C_g} \quad (3)$$

Equitation (3) indicates that by properly selecting the value of the feedback resistor Rf, small value of Q-factor can be achieved. The bandwidth is inversely proportional to the Q-factor of the circuit so, wide bandwidth can be achieved.

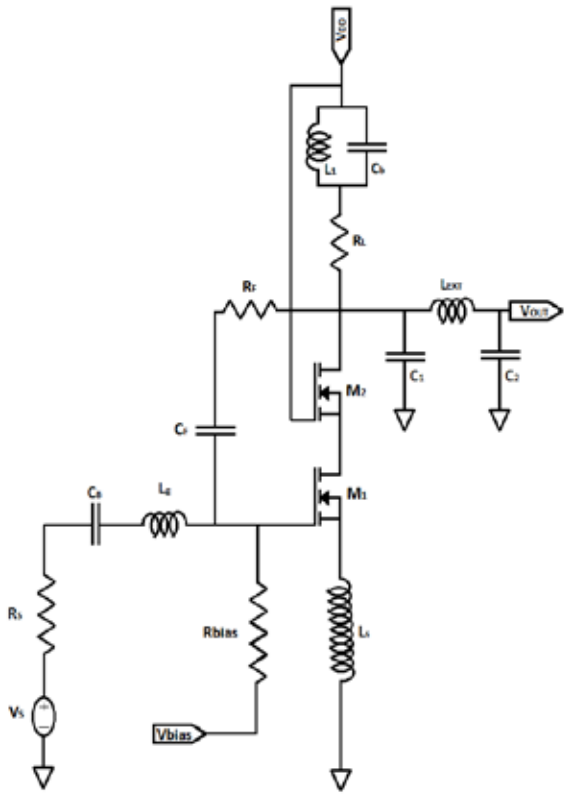


Figure:1. Schematic of Wideband LNA.

For $R_f >> R_s$, $R_f >> R_l$ and $g_m R_f >> 1$, the noise factor of the amplifier is given by

Volume : 2 | Issue : 1 | Jan 2013 • ISSN No 2277 - 8179

$$F > 1 + \frac{R_s}{R_f}\left[1 + \frac{1}{g_{m1}R_s}\right]^2 + \frac{\gamma}{g_{m1}R_s} \quad (4)$$

Where γ = 2 for short channel technique. From equation (3) and (4), it can be seen that the feedback resistor Rf is the key component to get the tradeoff between gain and noise figure.

III. Simulation Results

The CMOS wideband LNA with resistive feedback topology and bridge-shunt-series peaking network is designed to increase the gain and reduce the noise figure and power consumption using 0.13-µm CMOS technology. The supply voltage V_{dd} is 1.2V. For the evaluation, from figure 1(a), biasing node V_{bias} provides 0.6v to the gate of M_1 to operate it in the saturation. To operate M_2 in the saturation 1.2V applied to the gate of the M_2 through the V_{dd}.

The proposed LNA design is simulated using the SPICE software. Figure 2 shows the simulated gain of designed wideband LNA varying minimum 17dB over the frequency range 1 GHz to 8 GHz and maximum 25dB for higher frequencies above 6GHz.

Noise performance of the proposed LNA can be achieved in terms of Noise spectral density. Figure 3 (a), (b) shows the simulated noise spectral density in volts and dB's, respectively. The proposed LNA design provides the noise spectral density of -180dB (min).

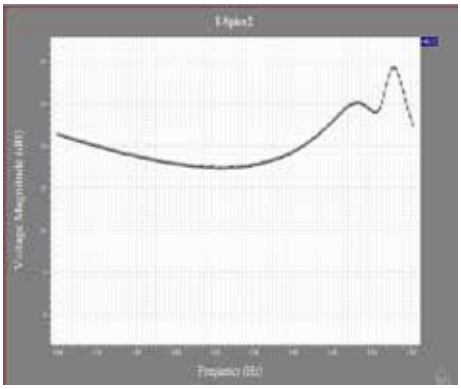
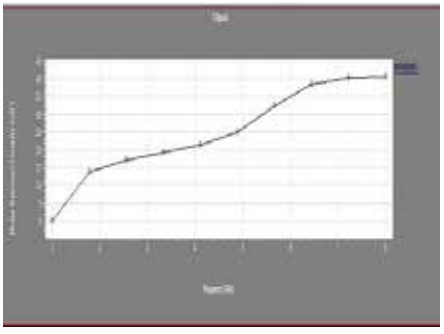
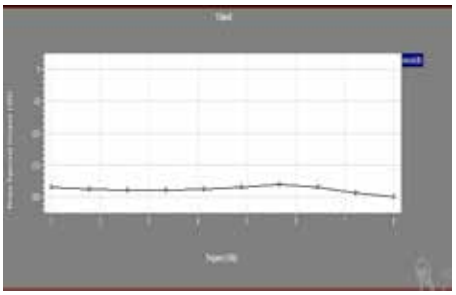


Figure:2. Simulated gain response of Proposed LNA.



(a)



(b)

Figure: 3. Simulated noise spectral density in (a) µv, (b) dB.

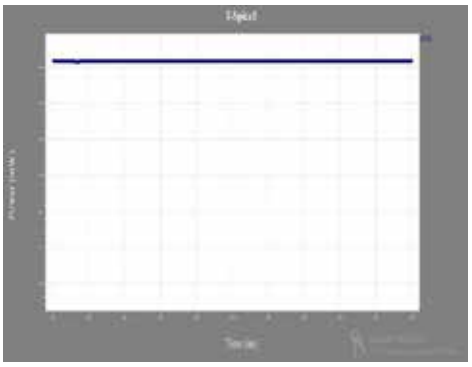


Figure: 4. Simulated power response of proposed LNA.

Figure 4 shows the power response of the proposed LNA design. The power consumption of the proposed LNA is 6.2mW. Figure 5 gives the physical layout of proposed design using microwind tool. Table II summarizes the measurement results which can be obtained by simulation.

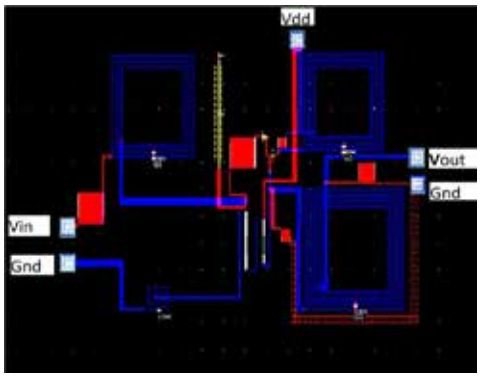


Figure: 5. Proposed Post layout of LNA.

TABLE II
Performance Summary

Technology	0.13-µm CMOS
Supply voltage	1.2v
Frequency	1-8GHz
Gain	17dB
Noise spectral density	-180dB
Power consumption	6.2mW

IV. Conclusion

A compact wideband LNA has been designed in 0.13-µm CMOS technology for wideband and low power application. The proposed LNA design uses the resistive shunt feedback topology with inductor degeneration topology. At the output side bandwidth can be extended using bridge-shunt-series network by dividing the load capacitance in two components. The amplifier achieved a bandwidth more than 7GHz, a gain of 17dB and better noise performance with lower power consumption of 6.2mW.

REFERENCE

[1] S. Shekhar, J. S. Walling, and D. J. Allslot, "Bandwidth Extension Techniques for CMOS Amplifiers," IEEE J. Solid-State Circuits, vol. 41, no. 11, Nov. 2006. | [2] Ke-Hou Chen, Jian-Hou Lu, Bo-Jiun Chen and Shen-Iuan Liu, "An Ultra Wide Band 0.4-10 GHz LNA in 0.18-µm CMOS," IEEE Trans. Circuits Syst. II: Express briefs, vol. 54, no.3, March 2007. | [3] Yi-Jing Lin, Shawn S. H. Hsu, Member IEEE, Jun-De Jin and C. Y. Chan, "A 3.1-10.6 GHz Ultra Wideband CMOS Low Noise Amplifier With Current Reused Technique," IEEE Microwave and Wireless Components Letters, vol. 17, nO. 3, March 2007. | [4] Qiang Li, Member, IEEE, and Yue Ping Zhang, "A 1.5 V 2-9.6 GHz Inductor-less Low Noise Amplifier in 0.13-µm CMOS," IEEE Trans. Microwave Theory and Techniques, vol. 55, no. 10, Oct. 2007. | [5] A. Meaamar, C. C. Boon, M. A. Do, and K. S. Yeo, "A 3–8 GHz lownoise CMOS amplifier," IEEE Microw.Wireless Components Lett., vol. 19, no. 4, pp. 245–247, Apr. 2009. | [6] K. H. Chen and C. K. Wang, "A 3.1-10.6 GHz CMOS Cascaded Two-stage Distributed Amplifier for UWB Application," IEEE Asia-Pacific Conference on Advanced System Integrated Circuits, August 2004. | [7] C. W. Kim, M. S. Kang, P. T. Anh, H. T. Kim, and S. G. Lee, "An ultra-wideband CMOS low noise amplifier for 3-5 GHz UWB system," IEEE J. Solid-State Circuits, vol. 40, no.2, pp. 544-547., Feb. 2005. | [8] Kambiz Moez and M. I. Elmastry, "A Low-Noise CMOS Distributed Amplifier for Ultra-Wide-Band Applications," IEEE Trans. Circuits and Systems II, vol. 55, no. 2, Feb. 2008. | [9] Bosco Leung, "VLSI for Wireless Communication", Prentice Hall Electronics and VLSI Series, pp. 75-89. | [10] B. Razavi, "Design of Analog Integrated CMOS Circuits", Mc-Graw Hill, 2001. |