Volume : 2 | Issue : 6 | June 2013 • ISSN No 2277 - 8179

Research Paper

Enhanced Power Gating Scheme for Low Leakage and Ground Bounce Noise

Engineering

KEYWORDS : Stack Power Gating, Diode power gating, stacked sleep approach

S. Guhan PG Student, Department of ECE, SRM University

U. Ragavendran Assistant Professor, Department of ECE, SRM University

ABSTRACT

Design of complex arithmetic logic circuits considering ground bounce noise, noise immunity, leakage current, active power and area is an important and challenging task in deep submicron circuits. A comparative analysis of high performance stacking power gating schemes is done which minimizes the leakage power and provides a way to control the ground bounce noise. The innovative power gating schemes such as stacking power gating diode based stacking power gating are analyzed which minimizes the peak of ground bounce noise in transition mode for deep submicron circuits. Further to evaluate the efficiency, the simulation has been done using such high performance power gating schemes. Leakage current comparison of NAND gate without power gating and with power gating scheme is done. Finally it is observed that the leakage current in standby mode is reduced by 87.14% over the conventional power gating. It is also found that in stacking power gating, the ground bounce noise has been reduced by 76.280/0 over the conventional power gating scheme. Finally, a detailed comparative analysis has been carried out to measure the design efficiency of high performance power gating schemes. This analysis provides an effective road map for high performance digital circuit designers who are interested to work with low power application in deep submicron circuits.

1. INTRODUCTION

The rapid progress in semiconductor technology, chip density and operation frequency have increased, making the power consumption in battery· operated portable devices a concern. High power consumption reduces the battery service life. The demand for portable electronic devices is growing rapidly and due in large part to the development of wireless communication, is expected to continue to grow. This demand has generated great interest in low power design. As the technology is reducing further day by day, contribution of leakage power in total power consumption has become comparable to or more than dynamic power consumption. For 180nm technology, it contributes only 10% of the total power while in 90nm technology it is comparable to dynamic power consumption, and for 45nm or technology less than this, leakage power is more the dynamic power. In battery operated devices, leakage power may cause serious problem, it reduces the battery life.

1.1 Stacking power gating Scheme:

A. Strategy to reduce leakage current in standby mode:

Here sleep transistors M 1 and M2 are stacked. When in standby mode i.e. When MI and M2 both are off. In this structure firstly, the leakage current is reduced by stacking effect, [1] turning both M 1 and M2 sleep transistors OFF. This raises the intennediate node voltage VGN to positive values to small drain current.

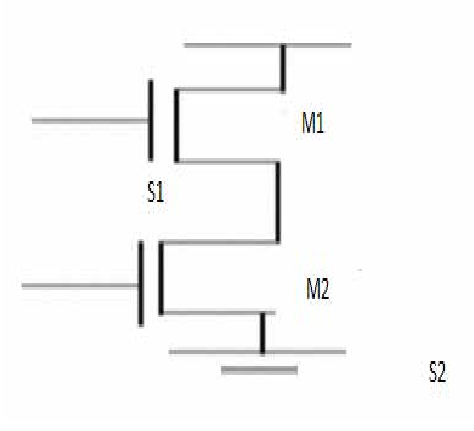

Fig-1: Stacking Structure

a) Gate to source voltage of M I (Vgs I) becomes negative
b) Negative body to source potential (Vbs I) of M1 causes more body effect
c) Drain to source potential (Vdsl) of M1 decreases, resulting in less drain induced barrier lowering
d) Drain to source potential (Vds2) of M2 is less compared to M1, because most of the voltage drops across M1 in sleep mode. This significantly the drain induced barrier lowering.

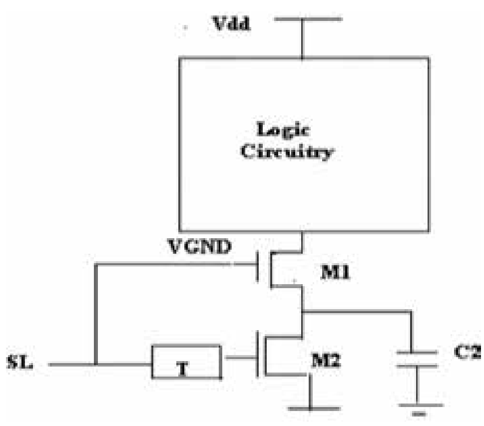

Fig-2: Stacking power gating

B. Strategy to reduce ground bounce noise:

a) Isolating the ground for small duration during mode transition.
b) Turning ON the M2 transistor in linear region instead of saturation region to decrease the current surge.

During sleep to active mode transition, transistor M I is turned ON and transistor M2 is turned ON after a small duration of time (IH) [1]. The logic circuit is isolated from the ground for a short duration as the transistor M2 is turned OFF. During this duration, the GBN can be greatly reduced by controlling the intermediate node voltage VGND2 and operating the transistor M2 in triode region. The intermediate node (VGND2) voltage can be controlled by

c) Inserting proper amount of delay that is less than the discharging time of the M1 transistor.
d) Proper selection of the capacitance C2.

C. Diode based Stacking Power Gating Scheme:

We can get more ground bounce noise reduction by incorporated strategy. Stacking sleep transistors (S1,S2) are used in diode based stacking power gating scheme shown in figure 2 reduce the magnitude of peak current and voltage glitches in power rails i.e. GBN. In the analyzed diode based stacking power gating scheme, the ground bounce noise is reduced by the following strategies.

Volume : 2 | Issue : 6 | June 2013 • ISSN No 2277 - 8179

a) Making the sleep transistor working as a diode during mode transition for some period of time due to this limitation in large transient hence reduction in the peak of GBN.
b) Isolating the ground for small duration during mode transition.
c) Turning ON the S2 transistor in linear region instead of saturation region to decrease the current surge.

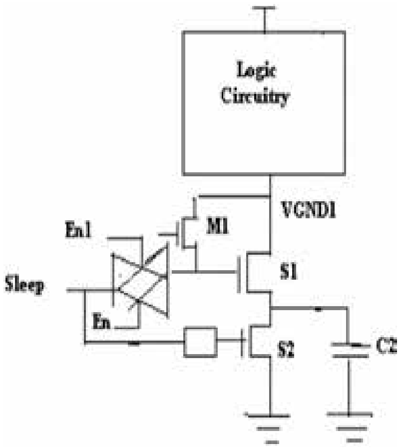

Fig-3: Diode stacking power gating.

Diode based Stacking power gating has three mode of operations

1. Active mode
2. Standby mode
3. Sleep to active mode transition and vice versa.

In active mode, the sleep signal of the transistor is held at logic' 1 ' and both the sleep transistors S1 and S2 remain ON and control transistor is OFF by giving logic O. In this case both transistors offer very low resistance and virtual ground (VGND) node potential is pulled [2] down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply Voltage. And leakage current is reduced by the stacking effect, turning both S1 and S2 sleep transistors OFF.

During sleep to active mode [2] transition, transistor S1 is turned ON and transistor S2 is turned ON after a small duration of time (6 T). The logic circuit is isolated from the ground for a short duration as the transistor S2 is turned OFF. During this duration, the GBN can be greatly reduced by controlling the intermediate node voltage VGND2 and operating the transistor S2 in triode region.

The intermediate node (VGND2) voltage can by

1. Inserting proper amount of delay, that is less than the discharging time of the S I transistor.
2. Proper selection of the capacitance C2.

Leakage current is reduced by the stacking effect, turning both SI and S2 sleep transistors OFF. This raises the intermediate node voltage VGND2 to positive values due to small drain current.

Positive potential at the intermediate node has four effects:

1. Gate to source voltage of SI (Vgs I) becomes negative Negative body- to- source potential (Vbs I) of S I causes more body effect.
2. Drain- to- source potential (Vdsl) of SI decreases, resulting in less drain induced barrier lowering

Drain-to-source potential (Vds2) of S2 is less compared to S I, because most of the voltage drops across the S I in sleep mode.

3. This significantly reduces the drain induced barrier lowering.

2. NOVEL STACKED SLEEP APPROACH:

While there are several process technology and circuit-level solutions to reduce leakage in processors, we propose novel approaches for reducing both leakage and dynamic power with minimum possible area and delay trade off.

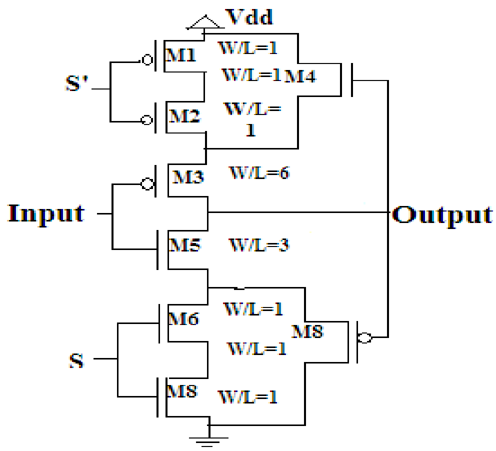

Fig-4: Novel stacked sleep approach

In this technique there are two sleep transistors is forcedly stacked in both pull-up and pull-down networks. So that we called it “Stacked Sleep” and maintaining the exact logic state, two extra transistors are used with the pull-up and pull-down networks. Basically the sleep transistor is used in this technique to reduce the leakage power in sleep mode. In this technique leakage is reduced in two ways, firstly stacked effect of sleep transistor and secondly, sleep transistor effect.

Sleep transistors induce extra internal resistance and according to the stack effect increases the channel length of the circuit. Sleep transistor is turned off when the exact generic logic circuit are not in use. Moreover sleep transistor isolated the logic network and that can help to reduce the leakage power dramatically during sleep mode. During active mode (Fig.)), s=1 and s'=O are asserted and thus all sleep transistors are turned ON. Since, the entire sleep transistors in pull-up network (M 1 and M2) and pull-down network (M6 and MS) are turned ON during active mode, so that circuit will perform faster. Furthermore, high Vth is used in this technique which can incur some delay penalty but reduces the leakage substantially. During sleep mode s=O and s'=1 are asserted and so all sleep transistors in both pull-up network (Ml and M2) and pull-down network (M6 and MS) are turned OFF. Although all sleep transistors are turned OFF but the circuit still maintains exact logic level by the help of two parallel transistors (M4 and MS). When sleep transistors are turned OFF, induce stack effect suppresses leakage power consumption. By combining this effect stacked sleep approaches can achieve low leakage. However its increase some delay penalty.

3. EXPERIMENTAL RESULTS:

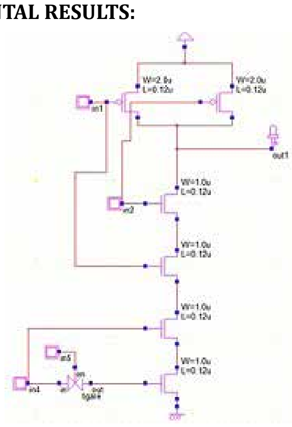

Fig-5: Stacking Power Gating

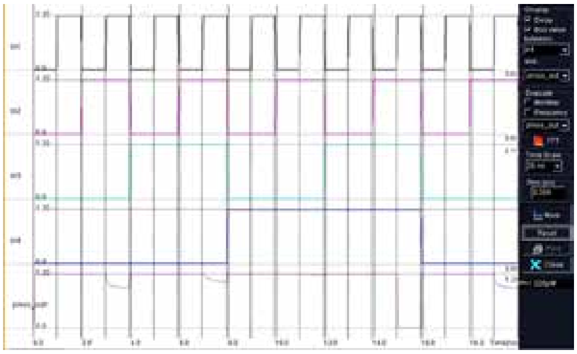

Fig-6: Output waveform for Stacking power gating

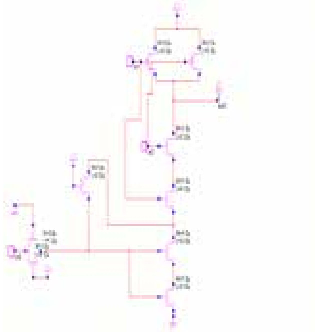

Fig-7: Diode stacking power gating

Here a high performance diode based stacking power gating structure has been presented which will minimize the leakage power as well control the ground bounce noise in transition mode .Diode stacking power gating technique has been analyzed and the conditions for the important design parameters Minimum ground bounce noise have been derived and its waveform is shown below

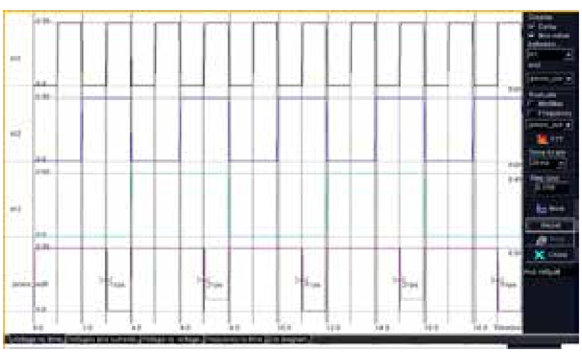

Fig-8: Diode Output waveform for Stacking power gating

3.1 Novel stacked sleep approach

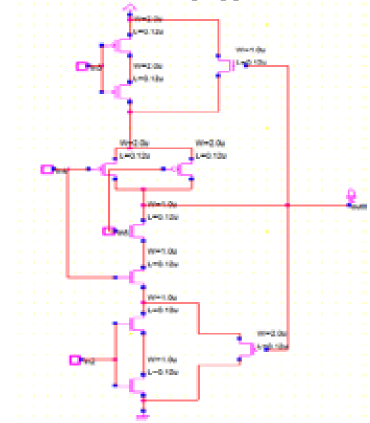

Fig-9: Novel stacked sleep approach

Novel stacked sleep approach technique has been analyzed and the conditions for the important design parameters minimum ground bounce noise have been derived and its waveform is shown below

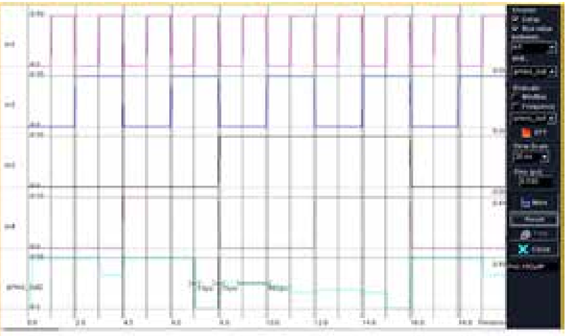

Fig -10: Output waveform of Novel stacked sleep approach

4. CONCLUSION:

In this method leakage current is reduced during the circuit sleep mode. However, the conventional power gating technique for minimizing leakage current introduces ground bounce noise during sleep to active mode transition. Stacking power gating technique has been analyzed and the conditions for the important design parameters. Minimum ground bounce noise have been derived. As recent trend is towards the nano-scale regime, power gating scheme is mostly used for reduction of leakage current. The ground bounce noise caused by the power gating structure is getting more prominent as the supply voltage is scaled down from 1.5V to 0.5V

REFERENCE

[1] Saxena, Chhavi ; Pattanaik, Manisha ; Tiwari, R. K. Devices,"Enhanced Power Gating Schemes for Low Leakage Low Ground Bounce Noise in Deep Submicron Circuits" International Conference on Digital Object Identifier: 10.1109/ICDCSyst.2012.6188736 Publication Year: 2012 , Page(s): 239 - 243 | [2] Kim Suhwan, S.V. Kosonocky, D. R Knebel, K. Stawiasz, M. e. Papaeftbymiou, "IEEE Journal of Circuit and systems II: Express briefs, pp. 586-590, 2007. | [3] Suhwan Kim, Chang Jun Choi, Deog- Kyoon Jeong, Kosonocky, Sung Bac Park, " Reducing ground bounce noise and stabilizing he data- retention voltage of power- gating structures" IEEE transactions on Electron Devices, vol. 55, pp. 197-205, June 2008. | [4] Shilpi Birla, Neeraj K. Shukla, Manisha Pattanaik and R. K Singh "Analysis of the data stability and leakage reduction in the various SRAM cells topologies", International Journal of engineering science & technology computer (HEST), Singapore, vol. 2(7), 2010, pp. 2936-2944, ISSN: 0975- 5462.