Implementation of a Fuzzy Logic Controller on an FPGA

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ABSTRACT   In this project fuzzy logic controller (FLC) will be implemented in VHDL for FPGA platform. This is a general purpose controller that can be used for different applications. This controller has three stages: the fuzzification, the inference and the defuzzification. The first component in the FLC is the fuzzifier that transforms crisp inputs into a set of membership values in the interval [0,1] in the corresponding fuzzy sets. The knowledge base of the fuzzy controller consists of a database of linguistics statements (rules), which states the relationship between the input domain fuzzy sets and output domain fuzzy sets. Inference block implements this logic. The last step is the defuzzification and the final output is determined by weighted average of all contributions of the output sets.

Modelsim Xilinx Edition (MXE) and Xilinx ISE will be used simulation and synthesis respectively. The Xilinx Chipscope tool will be used to test the FPGA inside results while the logic running on FPGA. The Xilinx Spartan 3 Family FPGA development board will be used this project.

1. INTRODUCTION:

Fuzzy Logic is a problem-solving control system methodology that lends itself to implementation in systems ranging from simple, small, embedded micro-controllers to large, networked, multi-channel PC or workstation-based data acquisition and control systems. It can be implemented in hardware, software, or a combination of both. FL provides a simple way to arrive at a definite conclusion based upon ambiguous, imprecise, noisy, or missing input information. FL's approach to control problems mimics how a person would make decisions, only much faster. A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by the customer or

Designer after manufacturing hence The FPGA configuration is generally specified using a hardware description language

(HDL), similar to that used for an application-specific integrated circuit (ASIC). FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial re-configuration of the portion of the design and the low non-recurring engineering costs relative to an ASIC design offer advantages for many application.

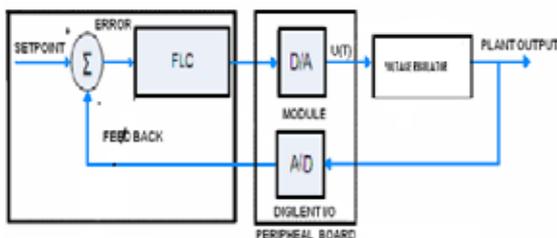**Layout of the proposed controller in a unity feedback control system:**

Fig 1.unity feedback control system

2. FUZZY CONTROLLER

The PI-like Fuzzy Logic Controller (PIFLC) has two inputs the error (e) and its change (Δe) and one output the change of control (Δu). This controller follows in its logic the three stages:
1) fuzzification,
2) inference and
3) Defuzzification.

We do remark that scaling factors can be introduced for input variables and the output one denoted respectively key, ked and kudu

3. FUZZIFICATION

The first component in the PIFLC is the fuzzifier that transforms crisp inputs into a set of membership values in the interval [0,1] in the corresponding fuzzy sets. The membership function shapes are typically triangular, trapezoidal or exponential.

Error (e) and its change (Δe) with fuzzy labels NB (negative big), NM (negative medium), NS (negative small), ZO (zero), PS (positive small), PM (positive medium) and PB (positive big). For the output, the membership functions are given in Fig. 8 and correspond to singletons in order to simplify the defuzzification process.

4. INFERENCE

The knowledge base of the fuzzy controller consists of a database of linguistics statements (rules), which states the relationship between the input domain fuzzy sets and output domain fuzzy sets. For a system with two inputs, the error (e) and change of error (Δe), and single output, each having seven fizzy sets, the rules can be represented in tabular form as shown in Table I. A maximum of 4 rules can be active at any time with triangular membership functions. The min-max inference method uses the min operator to find the minimum membership degree between the two inputs resulting from rule conditions and the rules are finally combined by using the OR operator and interpreted as the max operation for each possible value of the output variable.

5. DEFUZZIFICATION

The last step is the defuzzification and the final output is determined by weighted average of all contributions of the output sets. It is obtained by finding the centroid point of the function which is the result of the multiplication of the output membership function and the Inference output vector Y. The general mathematical formula which is used to obtain the centroid point

$$\Delta u = \frac{\sum_{i=1}^{5} Y[i] \times S[i]}{\sum_{i=1}^{5} Y[i]}$$

Y (i) are the i-th members of the output vector,

S (i) are the multiplying coefficients of the output membership function

6. ADC MODULE:

FPGAs are well suited for serial Analog to Digital (A/D) converters. This is mainly because serial interface consumes less communication lines while the FPGA is fast enough to accommodate the high speed serial data. The ADCS7476MSPS is a high speed, low power, 12-bit A/D converter. Consumes 80 ns time for one

cycle. A/D converter is a high speed serial interface that interfaces easily to FPGAs. The A/D interface adapter (AD1_PMOD) is implemented within the FPGA.

7. DAC MODULE:

The DAC121S101 is a dual, 12-bit voltage out Digital to Analog (D/A) converter. This device uses a versatile 6-wire serial interface that operates at a clock up to 20 MHz. The serial input register is 16 bits wide; 12 bits act as data bits for the D/A converter, It is interfaced to an FPGA as illustrated in Fig. 3. The D/A interface adapter (DAC_toplevel), which is implemented within the FPGA, facilitates parallel data input for the dual D/A converters

8. Chip Scope:

Chip Scope is embedded, software based logic analyzer. By inserting an "integrated controller core" (icon) and an "integrated logic analyzer" (ILA) into your design and connecting them properly, you can monitor any or all of the signals in your design. ChipScope provides you with convenient software

Based interface for controlling the "integrated logic analyzer," including setting the triggering options and viewing the waveforms.
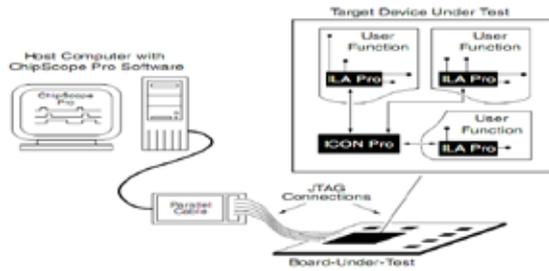

Fig 2. Chip Scope block diagram

9. Simulation Waveform:

Rst is used to reset the module or clear the previews data, clk is used for the synchronization, when the raising edge of clk is '1' then state is a counter go on counting from '0' to '16'count's. if count is '15' then data present in data1 &2 will be forced on to the shift resister's (signal's), if count is above '3' then data in

shift resister's will be forced on to output's from LSB to MSB till the count '15' by shifting 1 bit for each count. Sync_out and pclk will '1' for the count of "15".
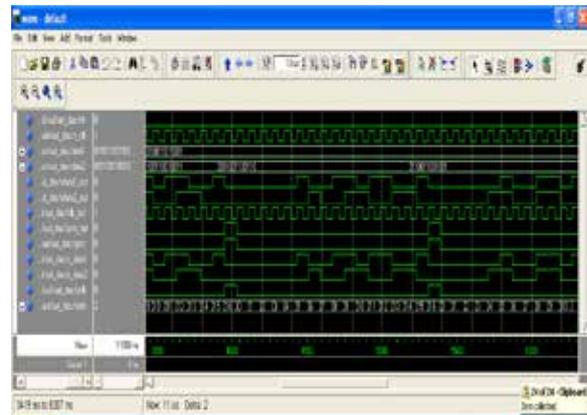

Fig 2. Simulation Results

CONCLUSION

This paper presents an approach for the implementation of a fuzzy logic controller on an FPGA using VHDL. A fuzzy logic controller with 2-inputs and 1-output is simulated and each block's verification is carried out using logic simulator. The FLC is implemented on a Xilinx Spartan-3 FPGA and used to control first order system to demonstrate its validity. The controller with the analog to digital and digital to analog interfaces was found to be fully functional. The FLC can also be used for control

Purposes in other applications. Also the length of input and output of the FLC can be increased to achieve better results.

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