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Research Paper

Error and Crosstalk Coding for CDMA On-Chip Communication Buses

Engineering

KEYWORDS : Network on Chip, Crosstalk avoidance, Multiple error correction.

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ABSTRACT

The communication requirements of large multiprocessor SoCs (MP-SoCs) can be conveniently met by the Network on Chip (NoC) paradigm. Network on Chip (NoC) is an enabling methodology of integrating a very high number of intellectual Property (IP) blocks in a single System on Chip (SoC). A major challenge that NoC design is expected to face is the intrinsic unreliability of the interconnect infrastructure. Some error may be occurring due to crosstalk and noise. In this project a simple coding scheme called Crosstalk Avoiding Double Error Correction Code (CADEC) is used for the application of CDMA bus in SoCs. The encoder is a simple combination of hamming coding followed by DAPS encoding to provide protection against crosstalk. In CADEC, the expected energy per bit will be less than in ED, as CADEC retransmits only when there are three or more errors compared to ED which retransmits even when there is a single error. Thus CADEC provides significant energy savings.

1. Introduction

Current commercial designs integrate from 10 to 100 embedded functional and storage blocks in a single system-on-chip (SoC), and the number is likely to increase significantly in the near future [2]. Network on chip (NoC) is viewed as a revolutionary methodology to achieve such a high degree of integration in a single SoC. According to the International Technology Roadmap for Semiconductors (ITRS) [10], signal integrity is expected to be an increasingly critical challenge in designing SoCs. The widespread adoption of the NoC paradigm will be possible if it addresses system level signal integrity and reliability issues in addition to easing the design process, and meeting all other constraints and objectives. With shrinking feature size, one of the major factors affecting signal integrity is transient errors, arising due to temporary conditions of the SoC and environmental factors. Among the transient failure mechanisms are crosstalk, electromagnetic interference, alpha particle hits, cosmic radiation, etc.[7].These failures can alter the behavior of the NoC fabrics and degrade the signal integrity. Providing resilience against such failures is critical for the operation of NoC- based chips.

There are many ways to achieve signal integrity. Among different practical methods, use of new materials for device and interconnect, and tight control of device layouts may be adopted in the NoC domain. Here we propose to tackle this

2 Data Coding in NoC Links

The common characteristic of NoC architectures is that the functional IP blocks communicate with each other via intelligent switches. The data communication between IP's in a NoC takes place in the form of packets routed through a wormhole switching mechanism. The packets are broken down into fixed length flow control units or flits. The transmitted flits are encoded to guard against possible transient errors.

On the other hand, incorporation of error correction codes makes the system more robust, so that the voltage level driving the system can be reduced without compromising bit error rates. This makes joint crosstalk-avoidance and error correction codes more suitable for lowering the energy dissipation of on-chip communication infrastructures.

There are a few joint crosstalk avoidance and single error correction codes (CAC/SEC) proposed by different research groups. Among these joint codes, the Dual Rail (DR) Code [23, 24] or Duplicate Add Parity (DAP), Boundary Shift Code (BSC) [22] and Modified Dual Rail Code (MDR) reduce the switching capacitance associated with crosstalk from (1+41) CL to (1+21) CL, where 1 is the ratio of the coupling capacitance to the bulk capacitance and CL is the load capacitance, including the self-capacitance of the wire. However, due to intensive integration and device shrinkage in the UDSM era, single error correction will not be sufficient to protect against different transient malfunctions. Hence there is a need for multiple error correction schemes. We propose a novel, simple joint crosstalk avoidance and double error correction scheme called crosstalk avoiding double error correction code (CADEC). We investigate the performance of CADEC in Comparison with the various existing joint CAC/SEC schemes in different NoC architectures. With increase in the correction capability of a code the probability of retransmission will reduce significantly. This will make energy efficient.

3. System Descriptions

3.1 Error Detection Code—EDC

This scheme implements Hamming code for error detection and retransmits if the scheme detects that the flit is in error [4]. As an example, the (38, 32) shortened Hamming code implemented for a 32 bit wide flit can reliably detect up to two errors in the flit. The ED scheme only detects the errors; on detection of any error pattern, it sends an automatic repeat request (ARQ) signal for retransmission of the flit. The encoder is essentially only a (38, 32) Hamming encoding block. The decoder is also a standard syndrome decoder for the Hamming encoded flit. Evidently, this scheme does not have any crosstalk avoidance properties.

3.2 DAP Schemes

The Duplicate Add Parity (DAP) scheme achieves joint crosstalk avoidance and single error correction capability by duplicating each bit of the n-bit flit and placing the copies adjacent to each other to avoid crosstalk, and by also computing a parity bit from the initial bits to enable single error correction. Thus, the encoded flit becomes 2n +1 bits wide [23, 30]. Where a second copy of the parity bit is transmitted to guard against crosstalk on the parity bit itself [26]. The encoder and decoder of the DAP scheme are shown in Fig. 1.

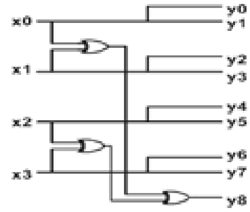

Fig. 1.a DAP encoder

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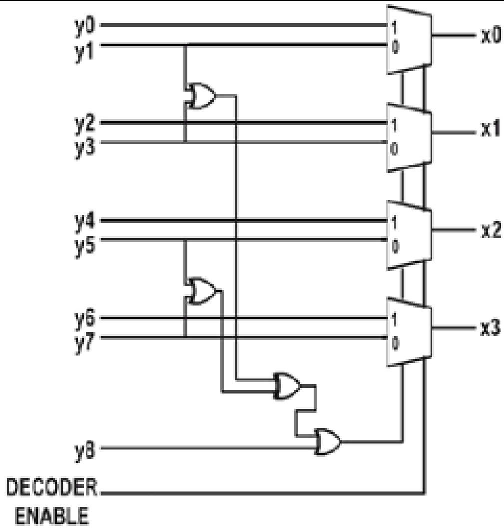

Fig. 1.b DAP decoder

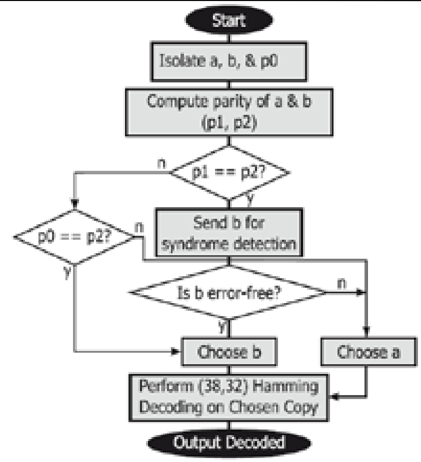

Fig.2 Decoding Algorithm for CADEC scheme

3.3 Crosstalk Avoiding Double Error Correction Scheme

Compared with Hamming codes, standard double error correction codes like BCH codes are computationally complex, and therefore are not very efficient from the perspective of energy reduction and area cost. In this work, we design a novel scheme which is capable of joint crosstalk avoidance and double error correction. We call this scheme CADEC coding. The encoder and decoder for the CADEC scheme are described in the following subsections.

Encoder: The encoder is simple combinations of hamming coding followed by DAP encoding to provide protection against crosstalk. As shown in Fig. 3a, the incoming 32-bit flit is first encoded using a standard (38,32) shortened Hamming code, then each bit of the 38-bit Hamming codeword is duplicated, and an overall parity calculated from one Hamming copy is appended. The (38,32) Hamming code has a Hamming distance of 3 between adjacent code words.

On duplication this becomes 6 and after adding the extra parity bit this distance becomes 7. A Hamming distance of 7 enables triple error correction, but at a somewhat higher complexity cost than the double-error correcting schemes considered here. Consequently, as a first step we considered only the double error correction capability. The extra parity bit, which is a part of DAP schemes is added to make the decoding process very energy efficient as explained below.

Decoder: The decoding procedure for the CADEC encoded flit can be explained with the help of the flow diagram shown in Fig. 2. The decoding algorithm consists of the following simple steps:

1. The parity bits of the individual Hamming copies are calculated and compared with the sent parity;
2. If these two parities obtained in step 1 differ, then the copy whose parity matches with the transmitted parity is selected as the output copy of the first stage.
3. If the two parities are equal, then any one copy is sent forward for syndrome detection.
4. If the syndrome obtained for this copy is zero then this copy is selected as the output of the first stage. Otherwise, the alternate copy is selected.
5. The output of the first stage is sent for (38, 32) single error correcting Hamming decoding, finally producing the decoded CADEC output.

The circuit implementing the decoder is schematically shown in Fig. 3(b).

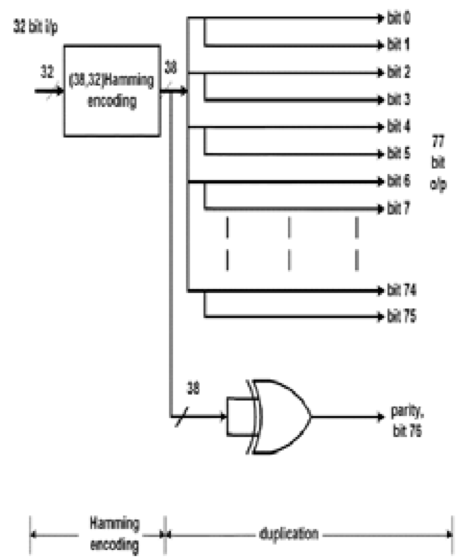

Fig. 3.a CADEC encoder

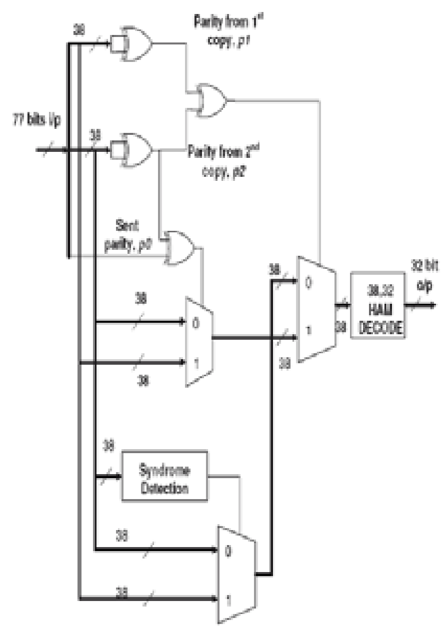

Fig. 3.b CADEC decoder

The use of the DAP parity bit effectively makes the decoder more energy efficient, compared to a scheme without the parity bit, which always requires a syndrome to be computed on both copies. When the parity bits generated from individual Hamming copies fail to match, the syndrome computing block need not be used at all, thus on average making the overall decoding process more energy efficient. This situation arises when there is single error in either one of the two Hamming copies, which, generally, will be the more probable case. We note that the circuit diagrams of Fig. 3 and the flowchart of Fig. 2 show only the logic for double error correction. To simultaneously detect triple or quadruple errors, one additional syndrome computation step must be performed on the copy selected for the final stage; if that copy has a non-zero syndrome, then there are three or more errors in the code word, and an ARQ request to retransmit the flit should be sent

4 Probability of Undetected Error

In the DSM NoC paradigm, reliability and energy dissipation cannot be decoupled. Enhancing reliability by performing coding invariably increases the energy overhead due to the codec blocks and redundant wires. But due to increased reliability, the voltage level driving the interconnect wires can be reduced without increasing the probability of residual word error, as the reduction in noise margin can be compensated by the increased error resilience [5]. Considerable energy savings can be achieved by reducing the voltage level on the interconnects, since the energy dissipation depends on the voltage squared. To quantify these gains, consider a Gaussian distributed noise voltage VN with variances 2 N which models the cumulative effect of all the transient DSM noise sources as mentioned before. This gives the probability of bit error, ε, also called the bit error rate (BER) as

$$\varepsilon = Q\left(\frac{V_{dd}}{2\sigma_N}\right) \quad (1)$$

Where the Q-function is given by

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^{\infty} e^{\frac{-y^2}{2}}\,dy \quad (2)$$

The word error probability is a function of the channel BER ε. If P_{unc} (ε) is the probability of word error in the uncoded case and P_{ecc} (ε) is the residual probability of word error with error control coding, then it is desirable that $P_{ecc}(\varepsilon) \le P_{unc}(\varepsilon)$ Using Eq. 1, we can reduce the supply voltage in presence of coding to , given by

$$\overline{V}_{dd} = V_{dd}\,\frac{Q^{-1}(\overline{\varepsilon})}{Q^{-1}(\varepsilon)} \quad (3)$$

In (3), V_{dd} is the nominal supply voltage in the absence of any coding. To compute for various schemes we find the residual word error probability for each of the schemes investigated in this paper.

4.1 Probability of Undetected Error for ED

As pointed out in [11], any (n, k) linear code can detect 2n − 2k error patterns of length n. The probability of undetected error for any (n, k) linear code can be computed from the weight distribution polynomial of the code, C (z), given by

$$C(z) = C_0 + C_1 z + \ldots\ldots + CnZ^{-n} \quad (4)$$

Where C_k is the number of codewords with weight (i.e.the number of 1s in the codeword) equal to k. The dual of the linear code also has an associated weight distribution, D(z), given by

$$D(z) = D_0 + D_1 z + \ldots\ldots + DnZ^{-n} \quad (5)$$

The weight distribution of the original code and its dual code are related by [11]

$$C(z) = 2^{-(n-k)}(1+z^n)D \quad (6)$$

The probability of undetected word error $P_{ED}(\varepsilon)$ for an error detection scheme using a linear code with dual weight distribution D(z) is [11]

$$P_{ED}(\varepsilon) = 2^{-(-n-k)}D(1-2\varepsilon)-(1-\varepsilon)^n, \quad (7)$$

where D(1-2ε) is given by

$$D(1-2\varepsilon) = \sum_{i=0}^{n} D_i(1-2\varepsilon)^i \quad (8)$$

The ED scheme proposed in [4] uses the (38, 32) shortened Hamming code for error detection, so the coefficients D_i in Eq. 8 are obtained by using the H-matrix of that code. Using Eq. 7, the probability of undetected error for the ED code, for small values of BER ε, turns out to be

$$P_{ED}(\varepsilon) = (n-k)\,\varepsilon^2 \quad (9)$$

where n =38 and k =32 for the (38,32) shortened Hamming code.

4.2 Probability of Undetected Error for DAP

The DAP coding scheme can correct all single error patterns and some multiple errors, which are taken into account while calculating the probability of undetected error. Let the original uncoded flit consist of k bits (we assume k =32 here). This makes the length of the DAP encoded flit to be (2k +1) bits. Correct decoding can happen under two circumstances as discussed below

1. The parity bit is error-free and one copy of the flit has no errors. The other copy in this case can have any number of erroneous bits. However, the parity has to be regenerated at the decoder only from the copy that is error-free. So, this possibility is not interchangeable between the two copies.

2. The other possibility for correct decoding is when the parity bit is in error. Then, if the (k+1)bits consisting of the copy from which the parity is regenerated and the sent parity have an odd number of errors, then the regenerated parity will not match the sent parity and the other copy which is error-free will be selected.

These two cases jointly give the set of cases where correct detection is possible, whose complement is the set of undetected errors. The probability of the set of undetected errors as computed in [30] is given by

$$P_{DAP}(\varepsilon) = \frac{3K(K+1)}{2}\varepsilon^2 \quad \mathbf{(10)}$$

4.3 Probability of Undetected Error for CADEC

The probability of correct decoding can be found by considering each of the cases where the decoder can correctly decode flits despite errors. The cases where the decoder can correctly decode words with more than two errors also need to be considered. The complement of the set of correctly decoded words constitutes the set of undetected errors. This probability is given by P_{CADEC} (ε). So, we have the relation:

$P_{CADEC}(\varepsilon) = 1 - P_{Correct}$ (11)

The complete probability of correct decoding, $P_{correct}$ is given by the sum of the probabilities corresponding to the above mutually exclusive cases. In the limit of small channel BER ε, this can be expressed as

$P_{Correct} = 1 - n^2(n-4)\,\varepsilon^3$ (12)

Using Eqs.11 and 12, the word error probability is

$P_{CADEC}(\varepsilon) = n^2(n-4)\,\varepsilon^3$ (13)

Using Eq.3, along with Eqs. 9, 10, and 13 for the undetected word error probabilities for the different coding schemes, the tolerable voltage swing reduction can be computed against varying values of BER ε.

5. Result and Discussion

In this work, we design a CADEC coding scheme which is capa-

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ble of joint crosstalk avoidance and double error correction. In the CADEC encoder incoming 32-bit flit is first encoded using a standard (38,32) shortened Hamming code, then each bit of the 38-bit Hamming codeword is duplicated, and an overall parity calculated from one Hamming copy is appended. The CADEC encoder output is obtained as 77 bit with one parity bit. The Total time delay for CADEC encoder part is 9.323ns. The detailed path delay of cadec encoder is shown in table 1.a and the simulation output image of cadec decoder are shown in figure 4.a

Table-1.a CADEC Encoder Delay

Logical name	Fan out	Gate delay(ns)	Net delay(ns)
Input buffer	6	1.106	0.721
LUT 4	2	0.612	0.532
LUT 2	1	0.612	0.509
LUT 4	1	0.612	0.387
LUT 4	3	0.612	0.451
Output Buffer	-	3.169	-
Total delay	9.323ns (6.723nslogic,.600ns route) (72.1% logic, 27.9% route)		

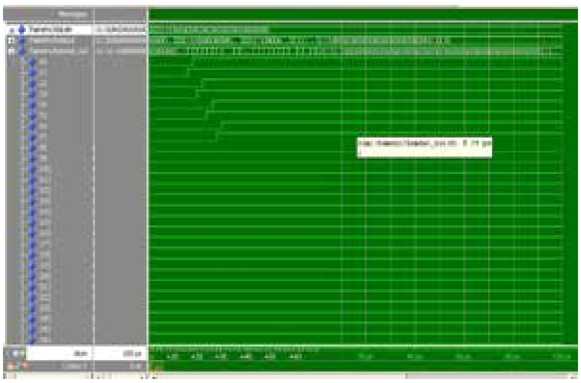

Fig 4.a CADEC encoder output

The CADEC decoder is consists of logic gates, multiplexer and hamming decoder. The incoming 77 bits with parity bit are first decoded into 38 bits and then it is given to input of the hamming decoder its further decoded the information bits and gives the 32 bit output.

The Total time delay for CADEC decoder part is 12.376ns.The detailed path delay of cadec decoder is shown in table 1.b.and the simulation output image of cadec decoder are shown in figure 4.b

Table-1.b CADEC Decoder Delay

Logical name	Fanout	Gate delay(ns)	Net delay(ns)
I/p buffer: I	2	1.106	0.532
LUT 2: I_0	4	0.612	0.529
LUT 4:I_2	6	0.612	0.638
LUT 4 : I_1	1	0.612	0.000
MUXF5: I_1	1	0.278	0.387
LUT 4: I_2	34	0.612	1.225
LUT 4: I_0	4	0.612	0.502
LUT 4: I_3	4	0.612	0.502
LUT 4: I_3	5	0.612	0.541
LUT 4: I_3	1	0.612	0.360
LUT 4: I_3	1	0.612	0.000
LD : D		0.268	
Total delay	12.376ns (7.160ns logic, 5.216ns route) (57.9% logic, 42.1% route)		

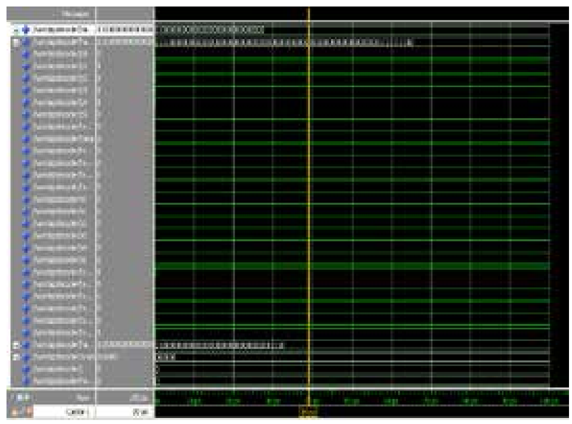

Figure 4.b CADEC decoder output

6. Conclusion

The communication requirements of large multiprocessor SoCs (MP-SoCs) can be conveniently met by the Network on Chip (NoC) paradigm. By incorporating joint crosstalk avoidance and double error correction coding, It correct 3 bit error if more than 3 bit error occur means retransmission occur. Thus the retransmission is significantly reduced. It is possible to simultaneously enhance the reliability of the NoC and lower the energy dissipation, despite the associated redundant wires and codec logic requirements. As verified through detailed analysis and simulations, the proposed CADEC scheme lowers the energy dissipation compared to all other existing schemes studied here. The energy savings arise from two factors, namely, the possibility of lowered voltage swing, and reduction of mutual switching capacitance of the inter-switch wire segments. From the analysis carried out in this work, it can also be concluded that coding schemes with higher order correction capability outperform sole retransmission-based mechanisms in terms of energy and area overhead.

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