Research Paper

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Logic Test of Single Cycle Access Structure

Engineering

KEYWORDS : Power testing, Test time reduction, Switching activity, Low power testing, At speed testing.

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ABSTRACT

This work proposes a new single cycle access structure for logic test. It not only eliminates the high power consumption and reduces the activity during shift and capture cycles. This leads to realistic circuit behavior during at-speed tests and stuck-at. This enables the complete test to run at higher frequencies equal or close to the functional mode. It shows that a lesser number of test cycles can be achieved by compared to other published solutions. The test cycles on a simple test pattern generator algorithm without test pattern compression is below 1 for larger designs and is independent of the design size. The structure allows additional on-chip debugging signal visibility for each register. The method is backward compatible to full scan designs and existing test pattern generators and simulators can be used with a minor enhancement. It is shown how to combine the proposed solution with built-in self test and massive parallel scan chains.

I.INTRODUCTION

The standard shift scan method is the most test implementation within for the decades. Automatic test pattern generation for sequential VLSI circuits is an NP-complete problem with an exponential complexity. The complexity of combinatorial logic varies. Less complex logic is tested within a few capture cycles, generating an immense number of don't cares during the rest of the test, even when test compression methods are used. Complex and hard to test logic needs to be stimulated and captured quite often but the pattern need to be shifted throughout the complete scan chain.

This work presents a novel scan cell register for logic tests combined with a novel scan cell routing architecture. The structure allows a single cycle access to individual register sets. This access scheme is fundamentally different to SS. It can be compared to a memory with single cycle synchronous write and asynchronous read functionality, whereas the remaining memory content (registers) does not change. The proposed structure is applicable for pattern driven tests and for BIST.

The paper provides reasonable data but is not limited to a frozen solution. It also discusses various trade-offs of different alternatives. Logic test is a wide field and different users have different preferences. A reference example based on 992 registers is used and should guide through the paper.

This becomes a major advantage during functional debugging of a chip embedded in a system or board, which is even more challenging. Almost all cases do not allow to rerun scenarios cycle accurate. Additionally, the failure could possibly appear only after a very long run-time. If the S-FF based chip fails on a board or within a system and must be debugged, register values can be shifted out but hardly accumulated to a continues waveform. The SCAhS has the same snap-shot capability but additionally allows continuous at-speed readout of one particular register line. This feature is sometimes embedded in the functionality but is now already implemented in the SCAhS and works for any set of SW registers. The continuously data stream can then be used by on-/off-chip trigger units or stored in waveform files. The asynchronous read feature of the SCAhS can become part of the chip's functionality. The SCAhS organizes the registers like a memory which can be read by a processor for instance. Also write cycles can be done if the remaining registers of a page accept a hold cycle by selecting page-select.

II. LITERATURE SURVEY.

Systematic Scan Reconfiguration- Ahmad A. Al-Yamani , Narendra Devta-Prasanna Arun Gunda in Proc. Int. Test Conf., 2008,Systematic Scan Reconfiguration,SSR is a compression solution that does not require any information about don't care bits. Yet, it achieves 10x to 40x reduction in test data volume, test application time, and tester channel requirements. With the same minimal hardware overhead as SAS, SSR achieves this major cost reduction through modifying the ATPG process instead of utilizing the don't care bits.

- Large volume of test data that must be stored in the testing equipment
- It increasingly long test application time
- It very high and still increasing logic-to-pin ratio creating a test data transfer bottleneck at the chip pins.

At-Speed Transition Fault Testing With Low Speed Scan Enable - Nisar Ahmed, C. P. Ravikumar, Mohammad Tehranipoor, Jim Plusquellic IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 24, no. 10, pp. 1594–1605, Oct. 2005,scan enables control information for the launch and capture cycle is embedded in the test data itself. A new scan cell, called the last transition generator (LTG), generates the local fast scan enable signals. The proposed method poses no additional constraints for the place and route tool and provides more flexibility to re-order the scan cells to meet the timing closure of the local scan enable signals.

- Reduce Power Dissipation
- Reduce The Scan-In Transition Probability.

Compression/Scan Co-design for Reducing Test Data Volume, Scan-in Power Dissipation, and Test Application Time- yu HUTa, Member, Yinhe HANT, student Member Xiaowei LI1, Huawei LIT, Nonmembers,and Xiaoqing WENT1, Member in Proc. 11th Pacific Rim Int. Symp. Depend. Comput., 2006,Our goal is to reduce all the VPT parts simultaneously. This is achieved by reducing test data Volume with variable-to-fixed run-1ength coding and reducing scan-in power dissipation as test application time with RAS structure.

- The increased power may reduce the life of batteries,
- Test application time and power dissipation.

Test Data Compression Based on Clustered Random Access Scan Yu Hu, Cheng Li, Jia Li, Yin-He Han, Xiao-Wei Li, Wei Wang, Hua-Wei Li, Proc. 15th Asian Tests Symp., 2006, a novel RAS architecture to reduce test data volume. The scan cells are clustered according to the compatibility of the test stimuli. To optimally cluster the scan cells, a heuristic clustering algorithm is employed. Then each cluster is assigned an address that can be uniquely accessed. Using address words rather than original patterns generated by ATPG, test data volume is significantly reduced. With less addresses assigned to clusters, the size of the address decoder and the number of global wires is reduced, thus smaller area overhead and routing overhead are achieved.

- Increasing Cost On Testing Due To Increased Complexity Of Test Generation And Large Volume Of Test Data.
- Energy, Peak Power, And Average Power During Testing Should Be Controlled To Avoid Causing Chip Malfunction And Reducing Reliability For Circuit-Under-Test (Cut).

III.PROPOSED SYSTEM.

This research proposes a new single cycle access test structure for logic test. It eliminates the peak power consumption problem of conventional shift-based scan chains and reduces the activity during shift and capture cycles. This leads to more realistic circuit behavior during stuck at and at-speed tests. It enables the complete test to run at much higher frequencies equal or close to the one in functional mode. It will be shown, that a lesser number of test cycles can be achieved compared to other published solutions. The test cycle per net based on a simple test pattern generator algorithm without test pattern compression is below 1 for larger designs and is independent of the design size. Results are compared to other published solutions on ISCAS'89 net lists. The structure allows an additional on-chip debugging signal visibility for each register. The method is backward compatible to full scan designs and existing test pattern generators and simulators can be used with a minor enhancement. It is shown how to combine the proposed solution with built-in self test (BIST) and massive parallel scan chains.

IV. METHODS AND SOLUTIONS

A. SINGLE CYCLE ACCESS STRUCTURE WITH HOLD MODE (SCAHS):

The key element of the single cycle access structure with hold mode (SCAhS) is the signal cycle access register with hold mode (SCAh-FF). It is based on a standard scan register (S-FF) and uses two more 2-to-1 multiplexers. The new SCAh-FF can be seen in Fig. 1.

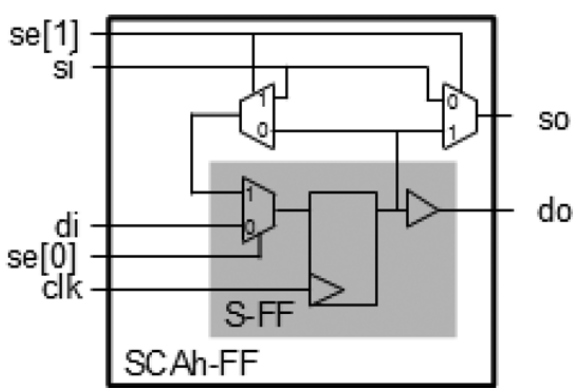

Figure 1: SCAh-FF.

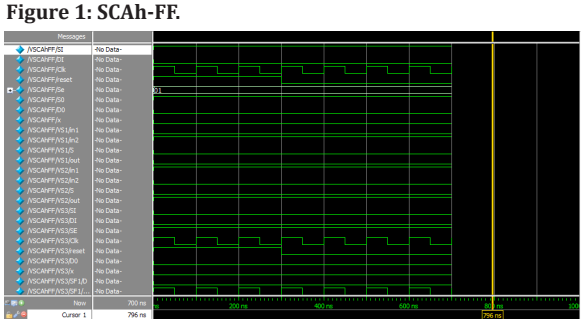

Figure 2: SCAh-FF OUTPUT.

The SCAh-FF has one more input and one more output compared to the standard shift register (S-FF). The inputs clock {clk}, data-in {di}, and scan-in {si} still exists. The scan-enable is now a 2 bit bus {se[0:1]}. An additional scan output pin {so} is added. The reset input and inverse output pins are not shown.

B. SCAH-FF CONNECTIVITY.

Figure.3 shows the SCAh-FF and its connectivity. The two major differences are, that the scan-in {si } is now connected to a dedicated scan-out {so } of the preceding register in the scan chain and the register { se[1]} inputs on the same scan depth are connected to the same line-select {ls } signal, which is driven by a "1 out of *N* " decoder. SCAh-FF connected to the same line-select signal are considered to be on one line.

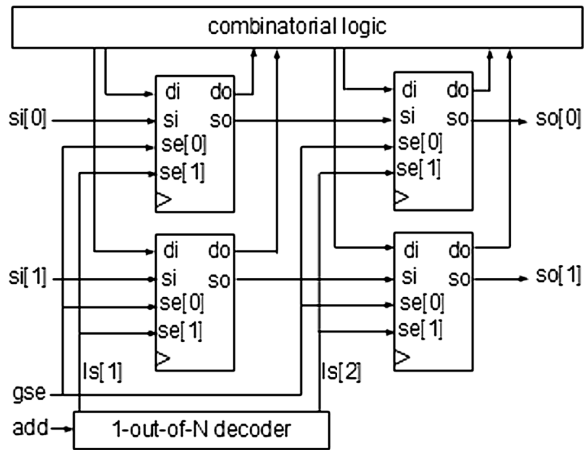

Figure 3. SCAhS connectivity.

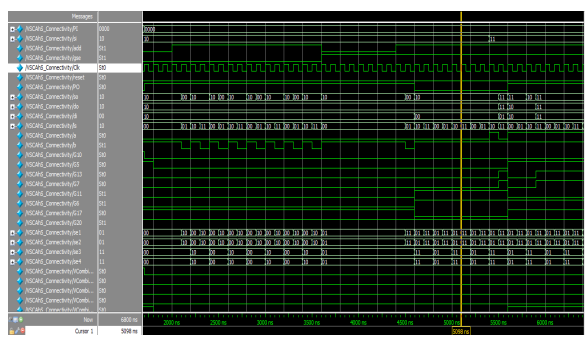

Figure 4. SCAhS connectivity OUTPUT.

If {add } is 0, no line is selected. { se[0]} of each SCAh-FF is connected to the global scan enable signal { gse} (comparable to the global scan enable signal of shift-scan structures). The output of the address decoder is connected to the {se[1] } pin of the registers on one particular line. Instead of shifting the data through the scan chain, all registers on the same scan depth, enabled by the same line-select signal can be read or written with a single cycle access.

C. SCA-STRUCTURE WITHOUT HOLD MODE.

In order to reduce the area overhead of a SCAhS, a simpler SCA-FF is discussed. It adds only one 2-to-1 MUX to the standard S-FF. It only has one {se} input, which is connected to the individual line-select signal. The pin which is connected to the global enable signal in the SCAhS is removed, so that the complete global scan enable tree becomes obsolete. The SCA-structure (SCAS) connectivity and page organization equals the one of the SCAhS without the global scan enable {gse}.

D.GATED SCA-STRUCTURE.

This section discusses the gated SCAS (gSCAS), which has all the benefits of the SCAhS but only has the area overhead of the SCAS. The hold function of the SCAh-FF is missing in the SCA-FF. It is instead built into the gated clock tree of the gSCAS. Fig shows the connectivity of the gSCA. The scan path reaches from the scan-in AND-selector over the SCA-FF chain (by connecting the scan-out pins of each SCA-FF with the scan-in pins of the succeeding SCA-FF) and is connected with the input of the XOR-tree. The individual line-select signals {ls} are connected with the {se } input of the SCA-FF in the relevant line.

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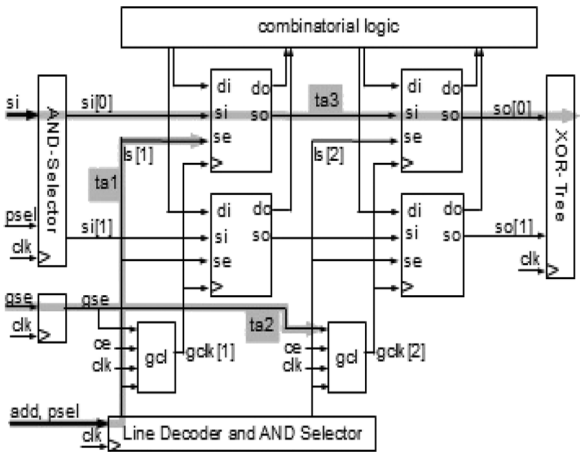

Figure. 5. gCAhS connectivity.

All SCA-FF on a line are clocked by a gated clock element (gcl). The gcl is driven by the clock and the line-select signal. The gated clock element can be enhanced, if a clock enable signal {ce } generated by combinatorial logic exists. The global scan enable signal is connected with each {gcl}, which is already the case in SS if gated clock elements are used to propagate the clock during shift.

E. SCAH-FF PAGE:

The SCAhS enables single cycle read/write accesses to the individual register line. The test structure is now organized in pages to achieve a read/write access at design speed or at a reasonable test speed. The page depth equals the scan chain depth (SD = number of SCAh-FF connected to one chain on one page). Assuming it is 31. Multiplied with the scan width (SW = number of scan chains on one page, for instance 32), the resulting number of SCAh-FF is SD*SW=992 per page.

V. IMPLEMENTATION.

Verilog HDL is a Hardware Description Language (HDL). A Hardware Description Language is a language used to describe a digital system, for example, a computer or a component of a computer. One may describe a digital system at several levels. For example, an HDL might describe the layout of the wires, resistors and transistors on an Integrated Circuit (IC) chip, i. e., the switch level. Or, it might describe the logical gates and flip flops in a digital system, i. e., the gate level. An even higher level describes the registers and the transfers of vectors of information between registers. This is called the Register Transfer Level (RTL). Verilog supports all of these levels. However, this handout focuses on only the portions of Verilog which support the RTL level.

Verilog is one of the two major Hardware Description Languages (HDL) used by hardware designers in industry and academia Verilog is very C-like and liked by electrical and computer engineers as most learn the C language in college. Verilog was introduced in 1985 by Gateway Design System Corporation, now a part of Cadence Design Systems, Inc.'s Systems Division. Until May, 1990, with the formation of Open Verilog International (OVI), Verilog HDL was a proprietary language of Cadence. Cadence was motivated to open the language to the Public Domain with the expectation that the market for Verilog HDL-related software products would grow more rapidly with broader acceptance of the language. Cadence realized that Verilog HDL users wanted other software and service companies to embrace the language and develop Verilog-supported design tools.

Figure. 6.TECHNOLOGY SCHEMATIC.

VI. CONCLUSION.

A single cycle access structure is discussed. Various implementations with and without hold mode as well as gated and partial implementation methods are presented. The aspects feasibility, peak power consumption, switching activity during test, area, test cycles, at-speed testing and debugging features are compared. A guide is given how to select the best implementation. The best solution (gSCAS) is compared to RAS implementations and is superior to all known RAS solutions. If BIST is preferable due to limited chip IOs or partial scan implementation, an address controlled BIST is discussed. The ATPG algorithms can be enhanced with the same methods SS implementations are optimized. Future work is related to algorithms for reducing the test cycles per net itself, register reordering, and pattern optimization for activity reduction and de-compression methods for BIST using the gSCAS.

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