

An Alternative Logic Approach to Implement Energy Efficient 90-Nm Cmos Full Adders



Engineering

KEYWORDS : Arithmetic, full Adders, low- power, power delay product, high speed, layout design.

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ABSTRACT

This paper presents power analysis of the seven full adder cells reported as having a low PDP (Power Delay Product), by means of speed, power consumption and area. In this we mainly present two proposed high-speed and low-power full-adder cells designed with an alternative internal logic structure and pass-transistor logic styles that lead to have a reduced power delay product (PDP). The existed standard full adders and the proposed full adders are designed and showed the better result comparison. This paper describes how the proposed full adders are better in contrast to the standard full adders. All the full-adders were designed with a 90-nm CMOS technology, and simulated using mentor graphics EDA tool with BSIMv3 (model49). Post-layout simulations show that the proposed full-adders outperform its counterparts exhibiting an average PDP advantage.

I.INTRODUCTION

Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation. In most of these systems the adder is part of the critical path that determines the overall performance of the system.

The amount of energy spent during the realization of a determined task relates to PDP and stands as the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies. The PDP exhibited by the full-adder would affect the system's overall performance. Thus, taking this fact into consideration, the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems.

In this paper, we report the design and performance comparison of two full-adder cells implemented with an alternative internal logic structure, based on the multiplexing of the Boolean functions XOR/ XNOR and AND/OR, to obtain balanced delays in SUM and CARRY outputs, respectively, and pass-transistor powerless/groundless logic styles, in order to reduce power consumption. The resultant full-adders show to be more efficient on regards of power consumption and delay when compared with other ones reported previously as good candidates to build low-power arithmetic modules.

II. PREVIOUS FULL-ADDER DESIGNS

Many papers have been published regarding the optimization of low-power full-adders, trying different options for the logic style (standard CMOS [1], differential cascode voltage switch (DCVS) [2], complementary pass-transistor logic (CPL) [3], double pass-transistor logic (DPL) [4], swing restored CPL (SR-CPL) [5], and hybrid styles [6]–[8]), and the logic structure used to build the adder module [9], [10]. The internal logic structure shown in Fig. 1 [11] has been adopted as the standard configuration in most of the enhancements developed for the 1-bit full-adder module. In this configuration, the adder module is formed by three main logical blocks: a XOR-XNOR gate to obtain A xor B and (Block 1), A xnor B and XOR blocks or multiplexers to obtain the SUM (So) and CARRY (Co) outputs (Blocks 2 and 3). A deep comparative study to determine the best implementation for Block 1 was presented in [12], and an important conclusion was pointed out in that work: the major problem regarding the propagation delay for a full-adder built with the logic structure shown in Fig. 1, is that it is necessary to obtain an intermediate A 8 B signal and its complement, which are then used to drive other blocks to generate the final outputs. Thus, the overall propagation delay and, in most of the cases, the power consumption of the full-adder depend on the delay and voltage

swing of the A 8 B signal and its complement generated within the cell. So, to increase the operational speed of the full-adder, it is necessary to develop a new logic structure that does not require the generation of intermediate signals to control the selection or transmission of other signals located on the critical path.

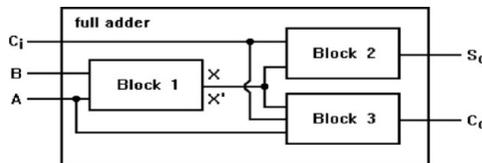


Fig.1.Full-adder cell formed by three main logical blocks.

III. ALTERNATIVE LOGIC STRUCTURE FOR A FULL-ADDER

Examining the full-adder's true-table in Table I, it can be seen that the So output is equal to the A xor B value when C=0 and it is equal to A xnor B when C=1. Thus, a multiplexer can be used to obtain the respective value taking the C input as the selection signal. Following the same criteria, the Co output is equal to the A.B value when C=0, and it is equal to A+B value when C=1. Again, C can be used to select the respective value for the required condition, driving a multiplexer. Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the A xor B and A xnor B signals, another block to obtain the A.B and A+B signals, and two multiplexers being driven by the C input to generate the So and C outputs, as shown in Fig. 2 [12].

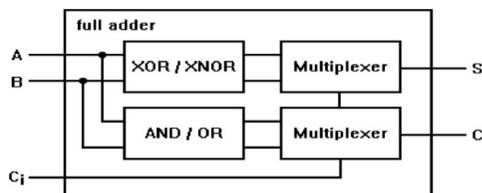


Fig. 2. Alternative logic scheme for designing full-adder cells.

C	B	A	So	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

True-Table For A 1-Bit Full-Adder: A, B, And C Are Inputs; So And Co Are Outputs

The features and advantages of this logic structure are as follows.

- There are not signals generated internally that control the selection of the output multiplexers. Instead, the C input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.
- The capacitive load for the C input has been reduced, as it is connected only to some transistor gates and no longer to some drain or source terminals, where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus, the overall delay for larger modules where the C signal falls on the critical path can be reduced.
- The propagation delay for the So and Co outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; this feature is advantageous for applications where the skew between arriving signals is critical for a proper operation (e.g., wave pipelining), and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications.
- The inclusion of buffers at the full-adder outputs can be implemented by interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NOR gates at the input of the multiplexers, improving in this way the performance for load-sensitive applications.

DPL Full adder

Two new full-adders have been designed using the logic styles DPL and SR-CPL, and the new logic structure presented in Fig. 2. Fig. 3 presents a full-adder designed using a DPL logic style to build the XOR/XNOR gates, and a pass-transistor based multiplexer to obtain the So output. In Fig. 5, the SR-CPL logic style was used to build these XOR/XNOR gates. In both cases, the AND/OR gates have been built using a powerless and ground-less pass-transistor configuration, respectively, and a pass-transistor based multiplexer to get the Co output.

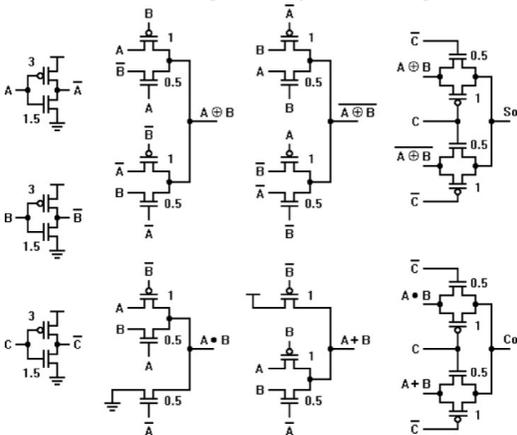


Fig. 3. Full-adder designed with the Proposed logic structure and a DPL logic style .

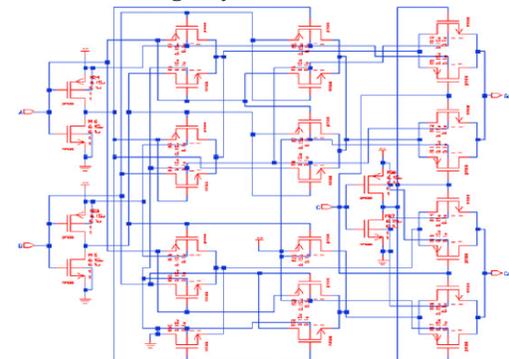


Fig.4 . Full-adder designed with a DPL logic style

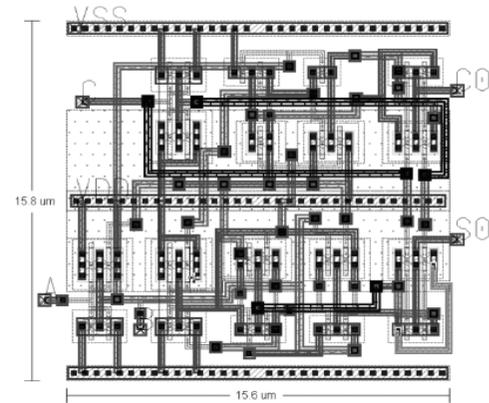


Fig. 5. Layout of the proposed dpl full-adder

SR-CPL full adder

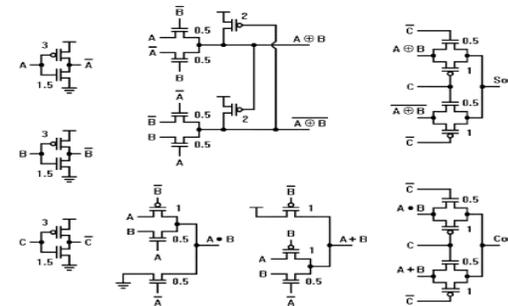


Fig. 6. Full-adder designed with the proposed logic structure and a SR-CPL logic style.

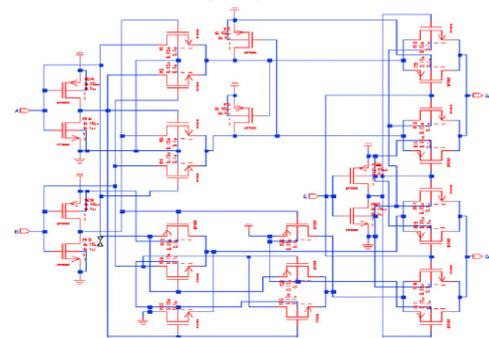


Fig.7. Full-adder designed with the SR-CPL logic style

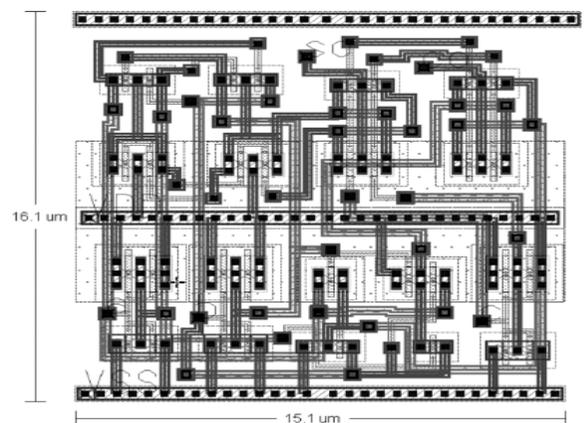


Fig. 8. Layout of the proposed sr-cpl full-adder

IV. SIMULATION ENVIRONMENT

The test bed used to simulate the full adders being compared is shown in Figure 5. This simulation environment has been commonly used to compare the performance of the full adders.

The advantage of using this test bed is that the Following power components are taken into account, besides the dynamic one: The short-circuit dissipation of the inverters connected at the full adder inputs.

This power consumption varies according to the capacitive load that the adder module offers at the inputs. Even more, the energy required to charge and discharge the full adder internal nodes when the module has no direct power supply connections (such is the case of pass transistor logic styles), comes through these inverters connected at the full adder inputs.

The short-circuit consumption of the full adder itself, as it is receiving signals with finite slopes coming from the buffers connected at the inputs, instead of ideal ones coming from voltage sources.

The short-circuit and static dissipation of the inverters connected to the outputs of the full adder due to the finite slopes and degraded voltage swing of the full adder output signals. The importance of including the effects and power consumption of the buffers connected at the inputs and outputs of the full adder cell come from the fact that the module is always going to be used in combination with other modules to build a larger system, and these static inverters are a good generalization for any other module to be considered.

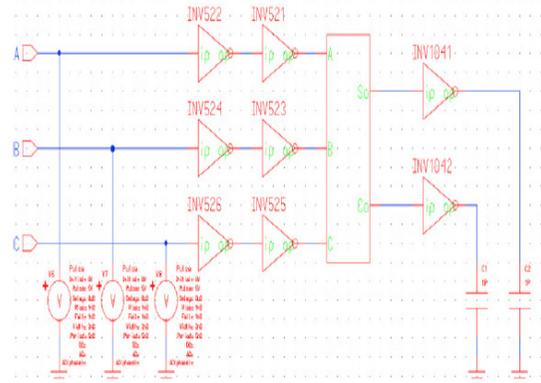


Fig. 9. Test bed used for simulating the full-adders under comparison.

V. SIMULATION RESULTS

We compared the performance of 7 full-adders, named: new14T [13], hpsc [6], hybrid [7], hybrid cmos [8], cpl [9], DPL and SR-CPL. The schematics and layouts were designed using a TSMC - 90 nm CMOS technology, and simulated using the BSIM3v3 model (model 49) and the post-layout extracted net lists containing R and C parasitics. Simulations were carried out using ICSTUDIO in Mentor Graphics Eda Tool. Table II shows the simulation results for full-adders performance comparison, regarding power consumption, propagation delay, PDP and area. All the full-adders were supplied with 1.8 V and the maximum frequency for the inputs was 200 MHz. This table reports the results for the whole test bed (top) and for the full-adder alone (add). It is worth to observe that in some cases, the power consumed from the power-supply (pwr supply) for the full-adder is smaller than the total average power (avg power).

TABLE II
SIMULATION RESULTS OF FULL ADDERS COMPARED (POWER IN W, DELAY IN PS, PDP IN W NS, AREA IN M², FREQUENCY IN GHZ AND V IN V)

schema		avg pwr	pwr supply	dynamic	static	short-circuit	% addtop	delay	PDP	area	F max	Vdd min
new14T	top	457.7	457.7	256.3	2.7	198.7	64.2	372	109.3	257	0.25	1.2
	fa	293.8	101.2	145.8	2.7	145.3						
hpsc	top	458.1	456.1	314.4	0.0	141.7	63.9	425	123.8	412	0.25	1.2
	fa	291.3	169.0	186.7	0.0	104.7						
hybrid	top	391.7	391.7	321.1	0.0	70.6	60.9	287	68.5	459	0.80	0.7
	fa	238.7	124.2	204.1	0.0	34.6						
hybrid_cmos	top	370.1	370.1	280.1	0.0	90.0	60.9	325	73.3	427	0.80	0.8
	fa	225.5	176.8	177.5	0.0	48.0						
cpl	top	265.1	266.1	183.6	0.2	82.3	54.6	284	41.3	378	1.50	0.6
	fa	145.3	135.7	103.7	0.2	41.4						
DPL	top	184.8	184.8	109.2	0.0	75.6	29.8	289	15.9	246	1.25	0.6
	fa	55.1	34.7	53.8	0.0	1.3						
SR-DPL	top	190.4	190.4	116.6	0.0	73.8	31.8	278	16.8	243	1.25	0.6
	fa	60.6	48.4	54.5	0.0	6.1						

From the results in Table II, we can state the following.

- Only two full-adders exhibit static-dissipation. These are the new14T and cpl adders, which are implemented with logic styles that have an incomplete voltage swing in some internal nodes, causing this consumption component.
- The power consumption improvements of the full-adders taken in descending order correlate with the optimizations reported in the correspondent papers. Considering the power consumption of the whole test bench, our proposals show savings up to 60%, and considering the consumption of the standalone full-adder the savings are up to 80%. These savings can be justified by the joint reduction of dynamic and short-circuit power components.
- With regards of the speed, it can be seen the advantage of the logic structure introduced here, since both realizations designed using this scheme (DPL and SR-CPL) exhibit the smallest propagation delay, only matched by the cpl full-adder. It shows a propagation delay improvement around 25% compared with the new14T and hpsc full-adders.
- The power-delay product (PDP) column confirms the energy-efficiency for the full-adders built using the new internal logic structure. They present the lowest PDP metric, up to 85% of saving, due to the combined reduction of power consumption and propagation delay.
- On regards of the implementation area obtained from the layouts, it can be seen that the proposed full-adders require the smallest area (up to 40% of relative area), which can also be considered as one of the factors for presenting lower delay and power consumption, as it implies smaller parasitic capacitances being driven inside the full-adder. The reason for the smaller area, compared to other full-adders that have less transistors, is that the size of the transistors in the proposed full-adders is minimal and not larger than 2x10⁻⁶ m (except for the symmetrical response inverters at the inputs), while for other full-adders the transistor sizes are in the range of 4 to 6x10⁻⁶ m. Figs. 8 and 9 show the layouts of the proposed full-adders, with the correspondent side by side dimensions.
- Finally, we determined the maximum frequency that each full adder can operate, while being supplied with 1.8 V. The proposed full-adders reach up to 1.25 GHz, only surpassed by cpl cell, at the expense of major power consumption and area. The reason for running the power-delay performance simulations at 200 MHz was due to the full adders that work only up to 250 MHz

VI. CONCLUSION

The design of high-speed low-power full adder cells based upon an alternative logic approach has been presented. MENTOR GRAPHICS EDA TOOL simulations have shown a great improvement on regards of power-delay metric for the proposed adders, when compared with previously published realizations designed with TSMC 90 nm technology, and were simulated and compared against other energy-efficient full-adders reported recently. Simulations showed power savings up to 80%, and speed improvements up to 25%, for a joint optimization of 85% for the PDP. The area utilization for the proposed full-adders is only 40% of the largest full-adder compared, and the power-supply voltage for the proposed full-adders can be lowered down to 0.6 V, maintaining proper functionality.

Some work can be done in the future on the design of 45 nm technology of high-speed low-power full adders but need to consider more DRC issues while going for the post layout simulation. And also the designs should be changed to achieve the required PDP levels of the standard and proposed full adders.

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