Diagnosis and Fault Tolerance for Embedded Bist RAMs

U.Siva Nagaraju — PG Student, Sathyabama university, Chennai. area of the project: VLSI Testing

Dr.A.sahaya Anselin Nisha — Assistant Professor, E&C department, Sathyabama university, Chennai.

ABSTRACT   *Due to poor controllability and observability of address, control and data lines embedded RAMs are extremely very difficult to test.the memory cell in embedded RAM have faults like stuck-at faults,coupling faults, data retention faults and bridging faults. To address this concern we developed a method which is used to detect the fault, isolate the location of the fault and can predict the remaining useful performance of embedded BIST RAMs.*

I . INTRODUCTION

As the use of systems increasing rapidly there is a necessity to check for any errors or faults with in a system so that the unexpected circuit failures in such systems may be prevented. The method "Diagnosis and Fault- Tolerant Control of Three-phase AC-dc PWM converter Systems" is used to detect the open switch faults that occur in a three-phase ac-dc PWM(pulse width-modulation) converter, and also it can minimize the imbalance of voltage ripple of the dc link and ac input currents in a three-phase ac-dc PWM converter.

The existing system[1] is very efficient to diagnose the open switch faults that occurs in any system, but it cannot diagnose the any other faults that are present in any systems. To address this concern we developed a a method "diagnostics and prognostics method" which is used to detect any faults like stuck-at faults,coupling faults, data retention faults and bridging faults. It not only detect the faults but also isolate the faults and predict the remaining useful performance of any circuits.

In order to find various types of faults we cosider an embedded BIST RAM architecture .the embedded memory built in self test(EMBIST) has the efficient structure which requires the smaller hardwawre. As current System-on-Chip(SOC) designs become memory in-depth, the manufacturing yield of such devices greatly depends on the yield of embedded memories. The embedded memory takes 80%~90% of the total SoC transistors and testing embedded memory has become a significant issue in developing SOC. Currently, the most widely used method for testing embedded memory is the Built-In Self-Test(BIST) method[2][3].

II.DIAGNOSTICS AND PROGNOSTICS METHOD

This method is implemented in two phases those are training and testing. During the training phase, The faults that are occurring frequently are explored in order to identify the faults of interest. EMBIST is then replicated for these hypothesized fault conditions and excited by a test stimulus to extract features that are stored in a fault dictionary for use during the online detection of faults. From the features that are extracted, an fault indicator(FI) is built whose trend is identified under different fault conditions. In the testing mode, the FI is calculated from the most recently extracted features.

A. Test signal generator:

For analog circuits, the behavioral characteristics are assumed to be embedded in the time and frequency response. Hence, a test signal must be chosen such that this response can be generated and captured. Most of the aforementioned ML-based diagnostic methods use a short pulse (typically 10μs) as a test signal. This process is done in order to obtain the impulse response of the CUT. By using this test signal generator[4], a high sampling rate and expensive data acquisition equipment are required to capture the response of the CUT, irrespective of the bandwidth of the CUT.
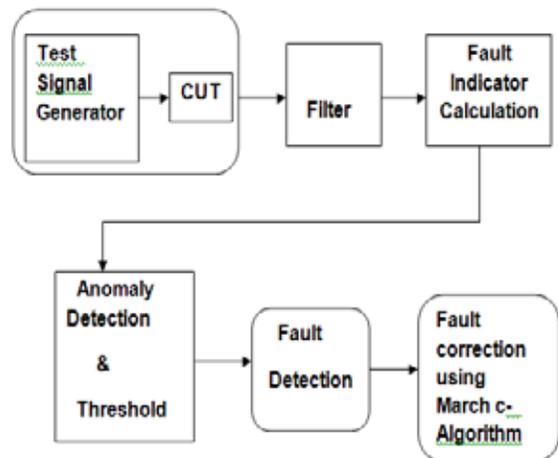

Figure 1: Frame work of diagnostics and prognostics method

B. Fault indication:

When implementing prognostics at the component level, usually a fault indicator (FI) parameter is identified to monitor the degradation of the component in real time. This parameter is chosen based on an understanding of the degradation process. For a complex system, multiple parameters corresponding to all the critical components/sub-systems need to be monitored and processed in real time to perform prognostics. This is not possible in applications such as analog circuits, where there is a constraint on the available resources. In order to address this challenge, we have developed a method to construct an FI to represent circuit degradation. Here, circuit degradation refers to the degradation in any of a circuit's critical components which leads to the deviation of the component's value from its nominal value.

C. Anomaly detection threshold:

A threshold for anomaly detection using the Mahalanobis Taguchi (MT) method is traditionally defined as Mahalanobis Distance (MD) 1. Here, in the calculation of the FI, an MD of 1 for both feature sets would result in an fault indicator value of 0.5. According to the MT method, the circuit is supposed to be displaying abnormal behavior when ever the FI value reaches 0.5. Through the experimental study the FI value is to be greater than 0.5, whenever a drifted outside the range of its tolerance. Thus, we chose the FI value of 0.5 as the threshold for anomaly detection.

D. Fault detection and isolation:

The fault detection and isolation problem is dealt with using an ML-based fault dictionary approach. During the training phase, the most likely fault conditions are first expected and Then, features are extracted from the circuit's response to the test signal under each of the fault conditions, which are emulated by seeding faults into the circuit. These features, along with the corre-

sponding fault conditions, form the fault dictionary. Here, the no fault condition is treated as a special form of fault condition and thus forms a separate class in the fault dictionary.

E. March c- algorithm :

March algorithms are known for memory testing because March-based tests are all simple and possess good fault coverage hence they are the dominant test algorithms implemented in most of the memory BIST in modern. The proposed march algorithm[5] is modified march c- algorithm which uses the concurrent technique. By the help of this modified march c- algorithm the complexity is reduced to 8n as well as the test time is reduced significantly. Because of concurrency in testing the sequences the test results are observed in less time than the conventional March tests. This technique is applied for a size 256x8 of memory and also can be extended to any size of memory. For testing purpose the functional fault models are modeled after faults in memories so that functional tests that detect these faults can be used. This modeling helps to simplify, clarify and generalize the testing approach of a memory. The quality of tests is strongly dependent on the fault model in terms of its fault coverage, its test length as well as the test time required. There are various fault models to test the functional faults such as stuck at faults; coupling faults are considered when it deals with SRAM. Address decoder faults and bridging faults will be considered when it deals with DRAM. Hence the most possible faults which occur in general are stuck at faults.

III.EMBEDDED BIST RAM ARCHITECTURE

The proposed structure of the memory BIST for testing the embedded memory is consisted of the following components. There is the EMBIST controller that generates the addresses and the control signals. And there is a pattern generator for generating data patterns. Also, it is composed of a response analyzer that compares the test results. The EMBIST controller controls the memory BIST, and generates the control signals that are needed during testing memories. In addition, the EMBIST controller generates the memory addresses in the memory tests. The pattern generator generates the data patterns during memory tests. The response analyzer compares between the output data and the expected data for determining if the faults exist or not. The Figure 2 shows this embedded memory BIST(EMBIST) architecture.
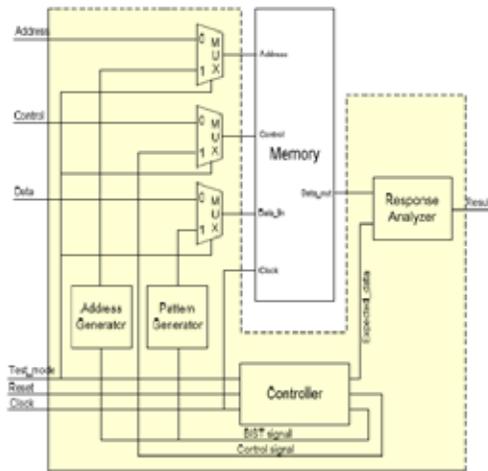

Figure 2: EMBIST Architecture

It is possible that EMBIST accomplishes more than one test algorithms, not only one algorithm. The test result has quite high fault coverage because the various plural algorithms can be selected. But, increasing the number of algorithms in EMBIST makes FSM bigger, and then it makes the hardware overhead larger.

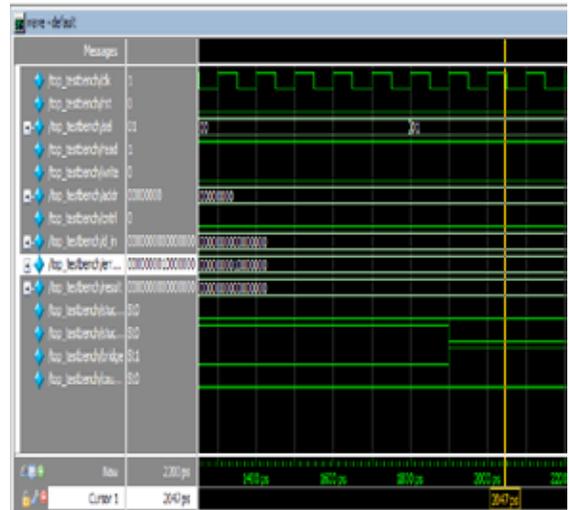### IV. RESULTS & DISCUSSION

Figure 3: Simulated Output

The above figure represents the output wave form of embedded BIST RAM. The faults like struck-at faults, coupling faults, bridging faults, etc... are calculated. If selection line is 00 both the struck at 0 faults as well as struck at 1 fault is detected. And selection line is 01 bridging fault is detected. And when the selection line is 10 the coupling fault is detected. Then the selection line 11 indicates there is no fault.

V.CONCLUSION

With the rapid growth of SOC (System-on-Chip), the BIST is being widely used to increase the yield of the built-in memories, which is a very important component in SOC. By using the separate on-chip test logic, the memory test can be performed to reduce the test time. Also it has the advantage of being able to detect the faults at system operation speed. Test methods for analog circuits like embedded RAMs have traditionally been developed to diagnose faults in the complex systems during the product development process. These test methods are not intended for the testing field operation, nor are they intended for predicting system failures due to circuit faults. But, the nature of the functions performed by mission or safety critical electronic systems demands methods that would enable the prevention of system failures due to faulty circuits. To address this concern, a method for the real time diagnostics and prognostics of analog circuits with an emphasis on early fault detection and failure prevention, has been presented.

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