Research Paper

Volume : 3 | Issue : 12 | December 2014 • ISSN No 2277 - 8179

Engineering

KEYWORDS : Gain-bandwidth product, CMRR, Phase Margin, Differential pair.

Design of Ultra Small Low Power High Performance Differential Amplifier Using CMOS in 70nm Technology

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ABSTRACT

At present, a high performance analog circuit using low voltage is strongly demanded. The differential amplifier is one of the most versatile circuits used in analog circuit design because of their excellent performance as amplifier and it is used in various applications. In this paper we have simulate a differential amplifier in 70nm CMOS technology which has high gain bandwidth product, low power dissipation. The phase margins, CMRR, output voltage swing are obtained for the circuit. In this paper we propose a new model of differential amplifier for high performance. This circuit is operated at 1.2v supply voltage.

1. Introduction of Differential amplifier

The differential amplifier is one of the most versatile circuits used in analog circuit design. These are widely used in the electronics industry and are generally preferred over their single-ended counterparts because of their better common-mode noise rejection, reduced harmonic distortion, and increased output voltage swing [3, 7]. It is also very compatible with integrated circuit technology and serves as the input stage to most of operational amplifier [13].

This paper deals with the designing and characterization of a low power high performance differential amplifier with active load and differential output. Section-II deals with basic and proposed differential amplifier. Design specification and the performance analysis are explained in section III. Simulation results are tabelized in section IV. Finally conclusion is drawn in section V.

2. Basic differential amplifier

Differential amplifier is designed to amplify the difference between two input signals. They can amplify a small difference between two signal levels and ignore any common level shared between them.[9]. In ideal differential amplifier the common mode gain should be zero and thus CMRR should be infinite, also the gain bandwidth product should be infinite [14, 6]. Practical differential amplifiers have non-zero common mode gain, therefore, the CMRR becomes finite and they have non-zero offset voltage [15]. CMOS differential amplifiers are used for various applications because a number of advantages can be derived from these types of amplifier, as compared to single-ended amplifier. The Differential amplifiers are used where linear amplification having a minimum of distortion is desired [4]. In Fig. a. shows the basic differential amplifier that uses N channel MOSFETs M3 and M4 to form a differential amplifier. M3 and M4 are bias with current sink I_{ss} connected to the source of M3 and M4. This configuration of M3 and M4 is often called a source coupled pair. The current sink I_{ss} is implemented using M1 and M2 [11].

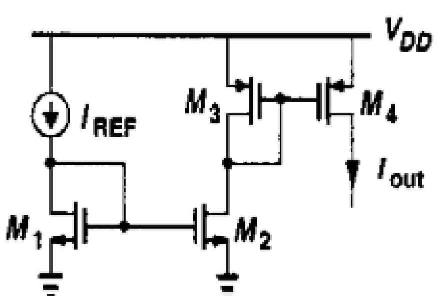


Fig. a Basic CMOS Differential Amplifier

The transistor M3 and M4 are perfectly matched and always worked in saturation region. The behavior of large signal analysis is given as [1, 2]:-

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}.$$

The design equation for differential amplifier

where $U_n C_{ox} = ß$ and $I_{ds1} = I_{ds1} - I_{ds2}$

$$I_{D1} = \frac{I_B}{2} + \frac{I_B}{2}\sqrt{\frac{\beta Vin^2}{I_B} - \frac{\beta^2 Vin^4}{4I_B^2}}$$

$$I_{D2} = \frac{I_B}{2} - \frac{I_B}{2}\sqrt{\frac{\beta Vin^2}{I_B} - \frac{\beta^2 Vin^4}{4I_B^2}}$$

Equation for Gain

$$A_v = \frac{V_{out}}{V_{in}}$$

$g_m = \sqrt{I_B \beta}$ The transconductance of the amplifer is

It is interested to note that as I_B is increased the transconductance also incerases

Equation for Power Dissipation

$$P_{diss} = V_{DD} I_5$$

Common mode rejection ratio

$$CMRR = \frac{A_{dn}}{A_{cn}}$$

Proposed CMOS Differential Amplifier

The proposed differential amplifier is shown in fig. b. this circuits provide better differential gain and very small common mode gain thus,the CMRR of the proposed amplifer is high the transistor M1 and M2 forms the input stage of differential amplifer and M3 and M4 are for the output stage transistor M5 and M6 are used for current sink and the transistor M8, M9, M10 and M11 are PMOS that are used as active load [5, 10].

It is difficult to fabricate resistors with tightly controlled values or a reasonable physical size. Consequently, it is desirable to replace rsistor wirh a MOS treansistor [8]. The differential input is applied between the gate terminal or control of M1 and M2 and the output can be taken across the drain of M3 and M4 [12]. The proposed differential amplifier structure is simulated W/L=2/1 and W/L=4/1 for NMOS and PMOS respectively in order to obtain the proper matching. Simulation in differential mode is

Volume : 3 | Issue : 12 | December 2014 • ISSN No 2277 - 8179

carred out by taking AC DC and Transient as input to gate terminal of M1 and the gate of M2 is in invert polarity.in order to analysis the common mode the gate of M1 and M2 is shorted and then the signal is applied for simulation.

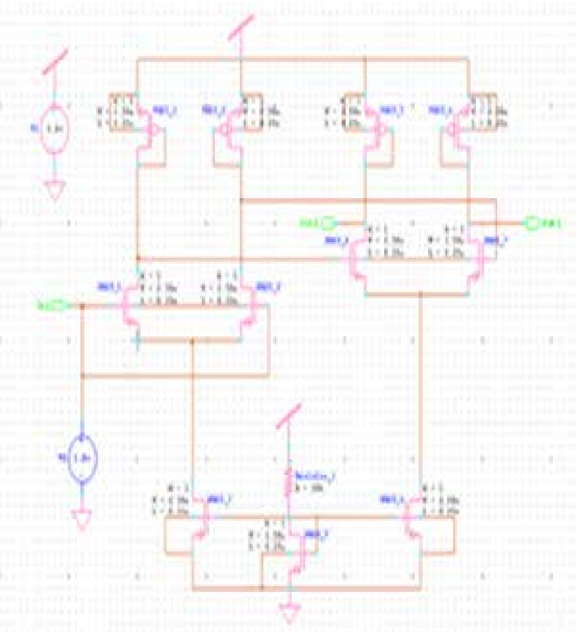


Figure b Proposed CMOS Differential Amplifier

3. Design specification and the performance analysis

The AC response for common mode and differential mode analysis as shown in fig. a. and b. This result shows the voltage gain, phase margin, CMRR and gain-bandwidth product. This result shows that the circuit works properly up to 7.35 MHz frequency. After this frequency the performance of the circuit is poor. The DC response shows the voltage transfer characteristics in common mode and differential mode configuration in fig. c. and d. The Transient response shows the output voltage swing in common mode and differential mode as shown in fig. e. and f. The wave form of common mode rejection ration is obtain by the AC analysis as shown in fig g.

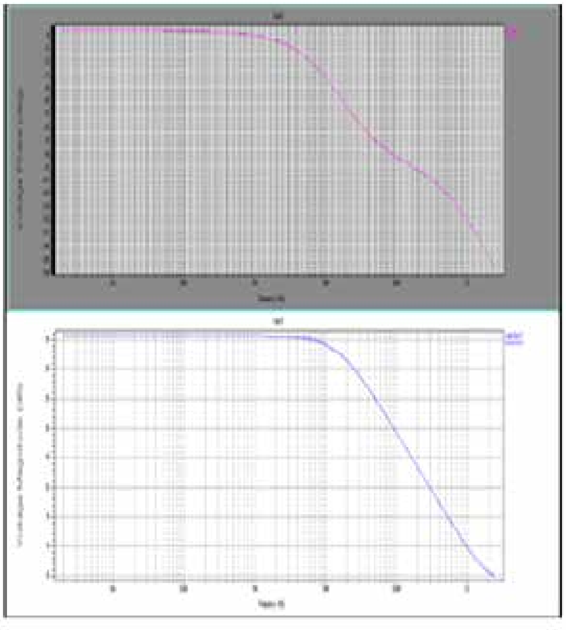


Figure. a. AC response obtained in differential mode.

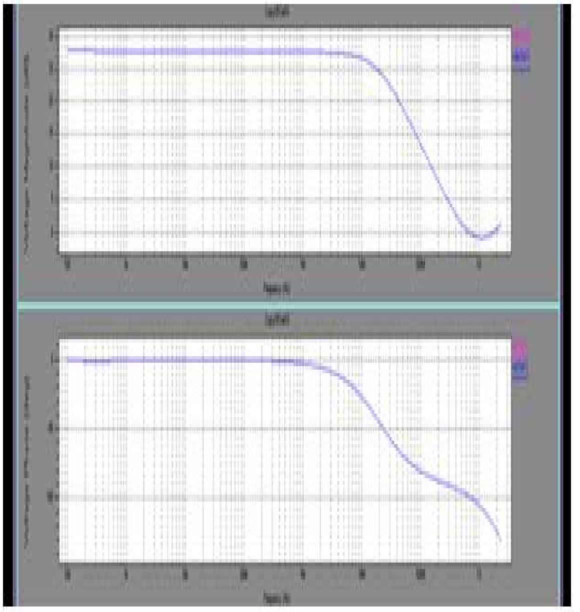


Figure. b. AC response obtained in common mode .

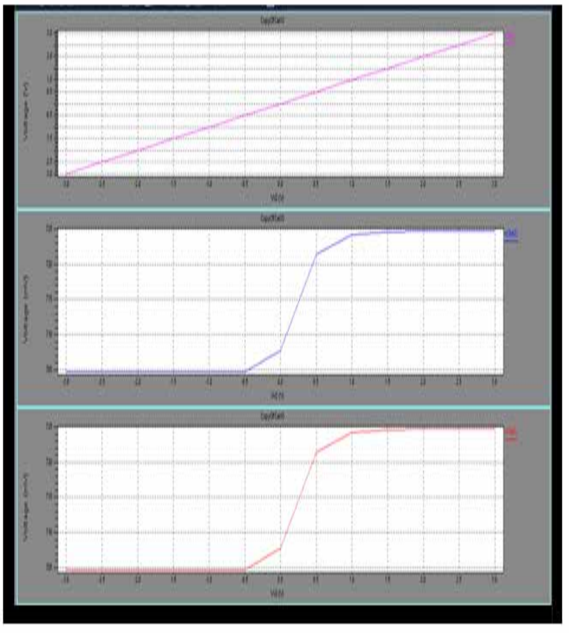
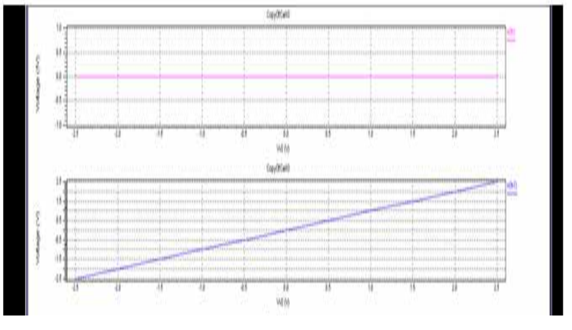


Figure. c. DC response obtained in common mode



Volume : 3 | Issue : 12 | December 2014 • ISSN No 2277 - 8179

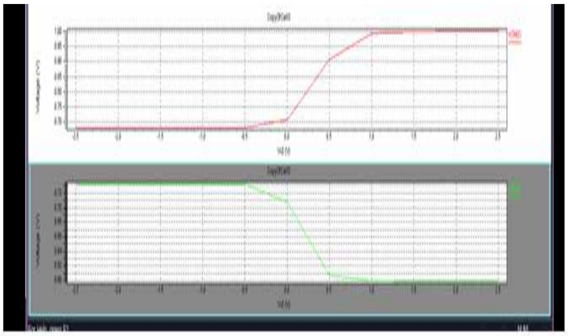


Figure. d. DC response obtained in differential mode

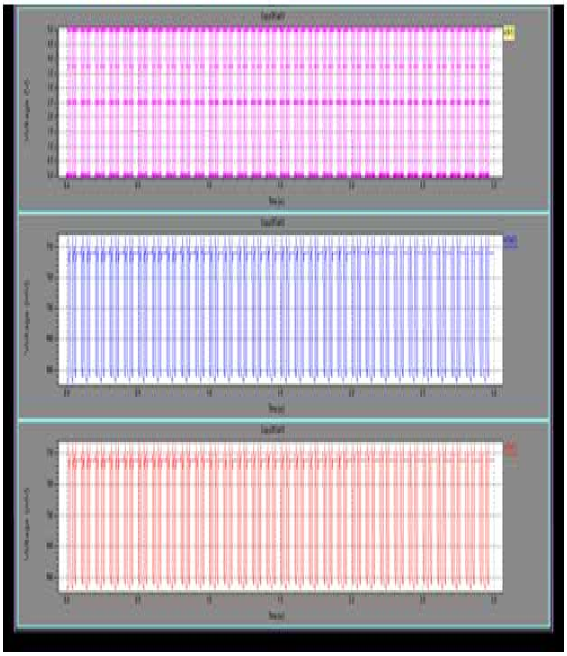


Figure. e. Transient response obtained in common mode.

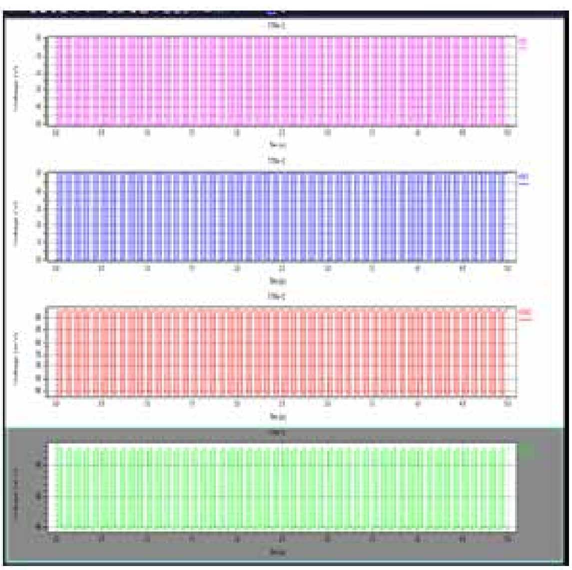


Figure. f. Transient response obtained in differential mode

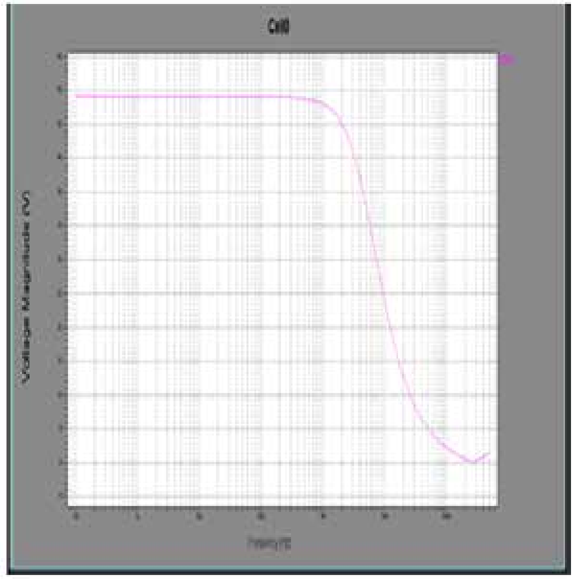


Figure. g. The waveform of CMRR with the help of AC analysis.

4. Simulation Results

Simulation results obtained using Tanner EDA Tool 14.11v for different analysis are summarized in Table-1

Table 1

Parameters	Ref.1	Ref. 2	Obtain Value
Channel Length	1um	1um	70nm
Supply Voltage	3.3V	3.14V	1.2v
Gain	40dB	-	36.4 dB
Gain-Bandwidth Product	41.78Mhz	-	795 MHz
Cut-off Frequency	100Khz	5Mhz	11.5 MHz
Phase Margin	-	-	62deg
CMRR	-	-	54.3dB
Power Dissipation	0.33mW	1mW	0.28mW
Output Voltage Swing	-	-	0.905v

5. Conclusions

In this paper a low power high performance differential amplifier using CMOS is designed and characterized. This circuit is suitable for low voltage and low common mode gain. The design is carried out using 70nm technology and supply voltage is 1.2v applied. For better performance we use PMOS load instead of resistive load. These circuits give the better result than the reference values. The obtain result are – CMRR 54.3db, phase margin 62 deg, gain bandwidth product 795 Mhz, gain 36.3db, power dissipation 0.28mW. The circuit can be used in design of low voltage operational amplifier, voltage controlled oscillators (VCO), Operational amplifiers.

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