Research Paper

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Novel Approach on Implementing IMA Computer for Airborne Application

Computer Science

KEYWORDS : IMA, LRU, CPM, PCIe, SRIO, VITA

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ABSTRACT

Airframers are trying hard to reduce the weight and power consumption for their new aircraft. Trend in avionics system architecture is towards general-purpose avionics computers, which are defined as platforms. A platform in itself is not performing any avionics function, but provides communication, computing and memory resources to the avionics (software) applications .This is something similar to a desktop PC providing a required resource (hardware, communication, memory, operating system services) to the applications. This paper presents how to implement the platform or common processing module an d establish the communication between the common processing modules (CPMs) as well as to the Input output(IO) Interface modules.

I. INTRODUCTION

The use of Integrated Modular Avionics (IMA) is rapidly expanding and is found in all classes of aircraft.IMA concept, which replaces numerous separate processors and line replaceable units (LRU) with fewer, more centralized processing units, is promising significant weight reduction and maintenance savings in the new generation of commercial and military airliners and simplifies the development process of avionics software and reduced cost.

II. IMA HARDWARE ARCHITECTURE

The heart of the IMA based computer architecture consists of common processing modules and IO Modules, with space reserved in the cabinet to add CPM and IO modules to accommodate future growth.The CPM and IO resources are shared using common back plane bus to move data between them.Common operating system and built-in utility software required for the IMA computer.

Figure 1 shows the how the CPM and IO modules are connected using common back plane bus.

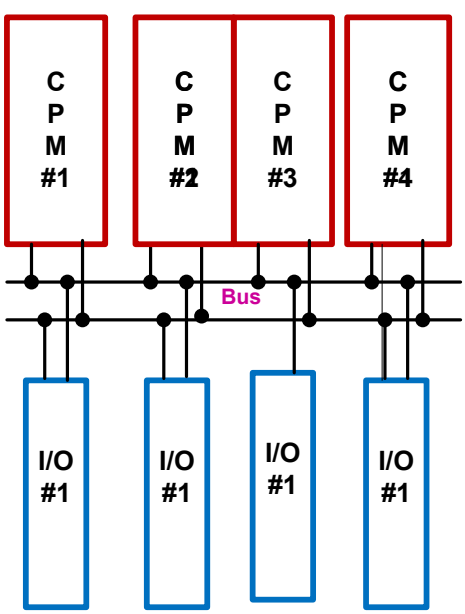

Figure1 General IMA Hardware Block Diagram

III.STANDARDS REQUIRED FOR IMA IMPLEMENTATION

The IMA computer architecture design must be reliable and robust.Inorder to achieve this, avionics standards such as ARINC653 for application portioning, industry standard such as VPX for hardware design needs to be followed as mentioned in the Figure 2.

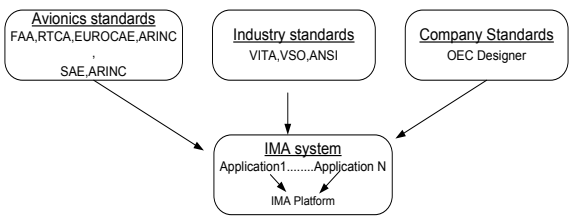

Figure 2. Standards required to implement IMA computer.

In order to design the hardware, the following Industry standard can be followed.

ANSI/VITA 46- VPX for Processing module design/back plane design, VITA 46.4, PCI Express on VPX Fabric Connector, VITA 46.3, Serial RapidIO on VPX Fabric Connector, VITA 46.7, Ethernet on VPX Fabric Connector, VITA 48 – VPX REDI for thermal plate design and ANSI/VITA 42 –for XMC module electrical and mechanical form factor.

IV.IMA COMPUTER ARCHITECTURE

The IMA computer needs to be designed using common processor module and IO module which can communicate using high speed serial interface.Depending on the computational requirement and application number of processing modules can be increased.Each processing module should be

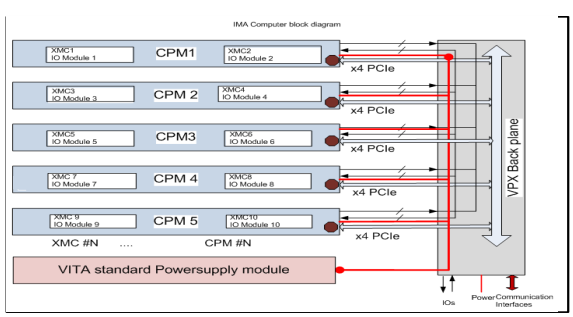

Figure 3: IMA Computer block diagram

designed to accommodate 2 mezzanine slots. Any IO requirement can be designed in the mezzanine module and which can be accessed by any processing module.The processing module to processing module as well as to the IO module communication can be using high speed serial interface such as sRIO and PCIe. The IO mezzanine module can be placed on any processing module which can be accessed using its geographical address. This architecture will address the single point failure. If one processing module fails and the IO module on it is healthy,other processing module should able resume its operation without affecting the application without affecting the performance.

V.COMMON PROCESSOR MODULE (CPM) DESIGN

Common processor module can be designed using commercially available System on chip(SoC) based processor which can be PowerPC ,intel , MIPS or arm core based architecture.The processor selection must be based on its performance such as number of floating point operations per second(FLOPS) and number of integer operations per second which can be measured as Million instruction per second,number pipeline stages, interface supports such as PCIe ,sRIO and Ethernet based high-speed serial interface(HSI) in addition to the memory interface and local bus interface . PCIe is required for communication with the IO Modules as well as to the other common processing module support.sRIO is required for CPM to CPM communication. Figure 4 shows how the Common processing module can be architected.

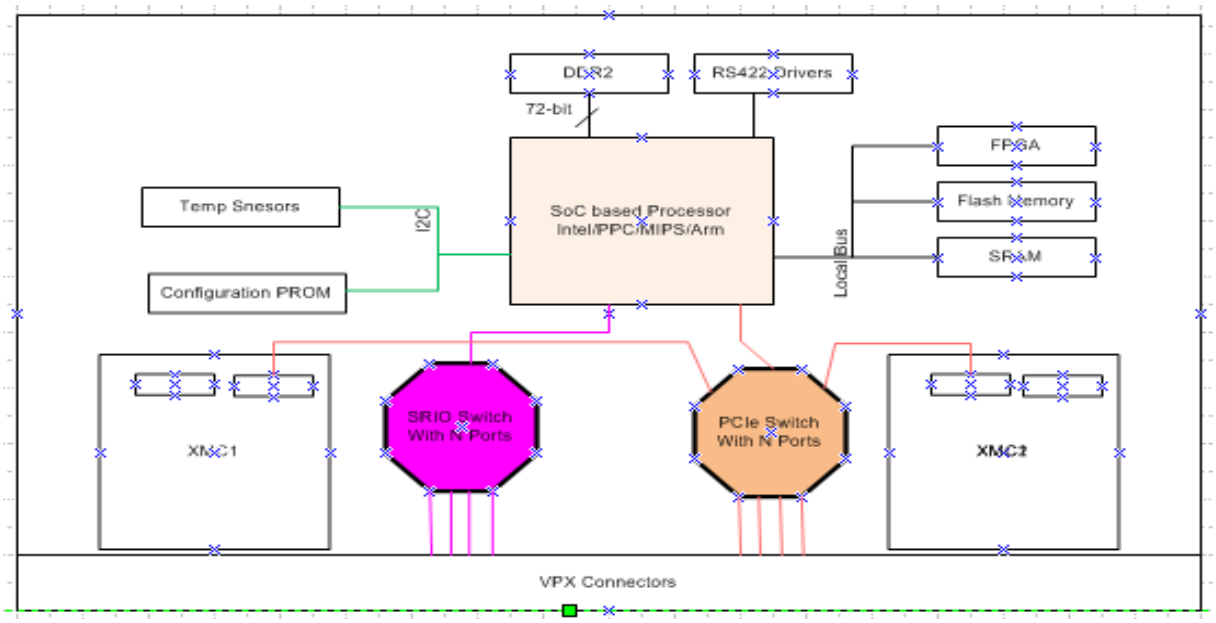

Figure 4 CPM architecture

VI.CRITICAL DESIGN PARAMETERS

Size, weight and Power (SWaP) needs to be considered during IMA computer design .Based on the ATR size, Number of slots needs to be decided.Power dissipation should be managed within the cooling method adopted.In addition to Swap, signal integrity of the High speed signal path needs to carried out. Based on eye opening and length supported on-board as well as on the back plane, accelerators on the high speed link can be decided

CONCLUSION

IMA based computer can be implemented using avionics standards, industry standards as well as the company standards. The design has to address the SWaP as well as the signal integrity. Proper attention is required while selecting the system on chip and implementation of the CPM.

REFERENCE

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