Research Paper

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Comparative Study of Area & Power Consumption Among Various Srams

Engineering

KEYWORDS :

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ABSTRACT

SRAM is designed to provide an interface with CPU and to replace DRAMs in system that requires very low power consumption. In present scenario battery –powered hand-held multimedia system have become popular. A SRAM cell must meet the requirements for the operation in submicron/nano ranges. The scaling of CMOS technology has significant impacts on SRAM cell- random fluctuations of electrical characteristics and substantial leakage current. Consequently, the static noise margin is degraded. This paper compares the read SNM and write SNM of 6T using noise voltage concept; read power consumption of 6T, 8T, 9T and 10T SRAMs and shows the area layout comparison among them using micro-wind tool. Simulations have been carried out using Tanner Tool at 180nm technology.

I. INTRODUCTION

The two very important aspects for SRAM cell design: the cell area and the power consumption of the cell. The cell area determines about two-thirds of total chip area. The power consumption is a factor which has to be minimized. Both of these aspects are inter-related because designing a cell for lower power consumption requires more number of transistors, i.e. larger cell area. SRAM (Static Random Access Memory) continues to be the most fundamental and important memory technologies today. Because of their fast, robust and easy manufacturing, they are nearly universally found on the same die with micro-controllers and micro-processors. Due to their higher speed, SRAM based cache memories and System-on-chips are commonly used. Device scaling has given rise to several design challenges for nanometer SRAM design.

Power and density have become the key limitations in many designs as nano-scaled devices are becoming reality at rapid pace. As the integration density of transistors increases, power consumption has become major concern in today's processors and SoC designs. The Dynamic power dissipation is due to the charging and discharging of load capacitances. CMOS circuits dissipate power by charging the various load capacitances whenever they are switched. The Short circuit power which occurs when there is a direct path from Vdd to ground, i.e. when both PMOS and NMOS are ON, is also a major source of power consumption in the digital circuits.

This paper focuses to compare the read SNM and write SNM of 6T using noise voltage; the area layout and read power consumption in 6T, 8T, 9T and 10T to show that there is a trade-off between area and power consumption.

II. CONVENTIONAL 6T SRAM CELL

SRAM bitcell is the basic building block of SRAM caches. Each bitcell stores one bit of information. The main parameters that should keep in mind while designing SRAM bitcells are bitcell area, speed, stability, power consumption and yield. Fig.1 shows the schematic diagram of conventional 6T SRAM bitcell.

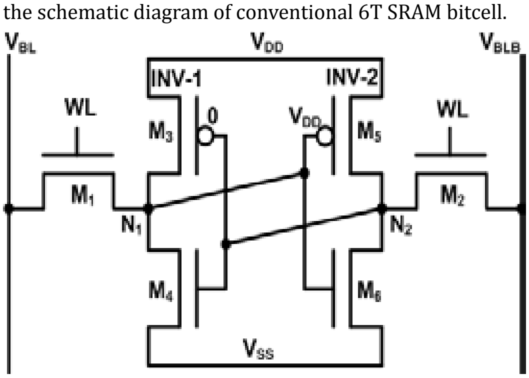


Figure1: Conventional 6T SRAM Cell

A conventional 6T-SRAM bitcell consists of two cross coupled inverters (INV1 and INV2) and access transistors (M1 and M2). The access transistors allow access to the data stored during read and write operations and provide isolation from other bitcells during hold state. Bitcells are accessed by asserting the word-line (WL) during a read or write operation by the access transistors.

A) Read operation

Fig.2 shows the 6T SRAM equivalent schematic diagram during read operation. Bit lines are precharged to supply voltage before read operation. The read operation is initiated by enabling the word-line (WL) and thereby connecting the internal nodes of the SRAM bitcell to bit-lines. The bit line voltage is pulled down by the nMOS transistor at the '0' storage node and the difference between two bit line voltages will be detected by sense amplifier. When the word line(WL) is high, one of the bit line voltages is pulled down through transistors M2 and M6 or M1 and M4. The transistors M2 and M6 forms a voltage divider, because of current flowing through M2, the potential at node QB is no longer at '0'V. Also it should not go beyond switching threshold of inverter (INV1) to avoid destructive read. The rising of potential depends on sizing of access transistor and pull down transistor which is defined as a bitcell ratio.

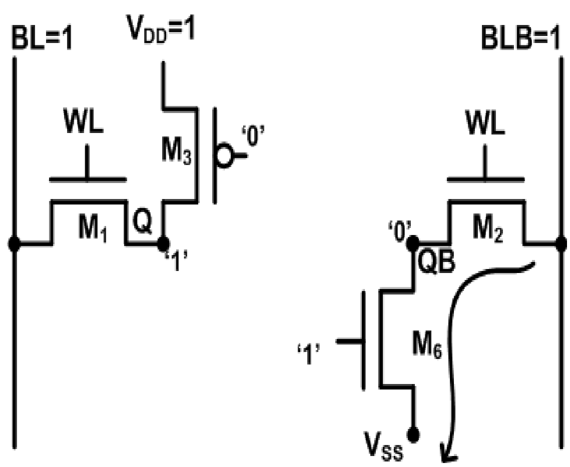


Figure2: Read Equivalent of 6T

B) Write operation

The write operation begins by forcing a differential voltage (VDD, and 0) at the bitline pairs (BLB and BL). This differential voltage corresponds to the data to be written at the storage nodes (Q and QB) and it is controlled by the write drivers. The WL is then activated to store the information from the bit-line pairs to corresponding storage nodes. Assume, the nodes Q and QB initially store values '1' and '0' respectively. When the WL is asserted the access transistor (M1) connected to BL (at '0') is turned on, a current flows from VDD to BL through M3 and M1. This current flow lowers the potential at Q. The potential at the node Q has to go below the trip point of the inverter (INV2) for a successful write operation and this depends on the ratio of pull-up transistor (M3) and the access transistor (M1). This ratio is referred to as the pullup- ratio.

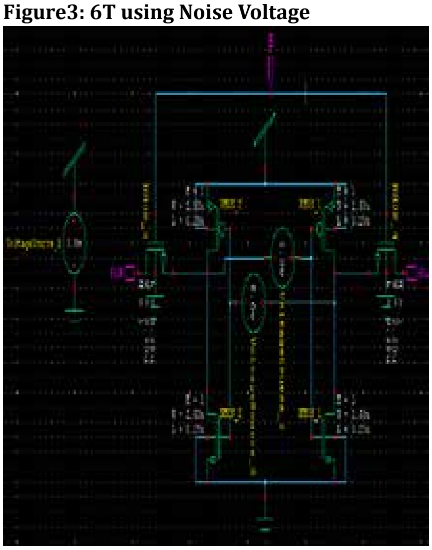
C) Hold operation

When WL goes low, SRAM bitcell is in data retention mode. Two cross coupled inverters hold the data, through bistable action. There is destruction in data stored when VDD goes below certain voltage, which is called data retention voltage of SRAM bitcell. A standard 6T SRAM shows poor read stability as technology scale down to nano-regime. To increase the read stability (measured by read SNM) conventional device sizing can be followed by increasing the bitcell ratio. By increasing the bitcell ratio, read SNM and critical charge (node capacitance) will increase which are desirable. However, at the same time power consumption and write time increases which are not desirable features, as they incur loss of power, performance and increase in area overhead. In Table I it is shown that when we are increasing the bitcell ratio there is significant increase in write time, which will affect the performance of SRAM bitcell.

III. READ SNM AND WRITE SNM OF 6T SRAM

Static noise is dc disturbance such as offsets and mismatches due to processing and variations in operating conditions [1]. The SNM is defined as the maximum value of noise voltage that can be tolerated by the cell before changing the contents. Figure3 shows the schematic of 6T SRAM cell using two noise sources.

Figure3: 6T using Noise Voltage



A) Read operation:

If we take the noise voltage to be 0.42V in the beginning of read operation where BL is storing '1', then the following waveforms (figure4) of BL (bit-line) and BLB (bit-line bar) and corresponding node voltages Q and Qbar (figure5) will be obtained.

Figure4: waveforms at BL and BLB

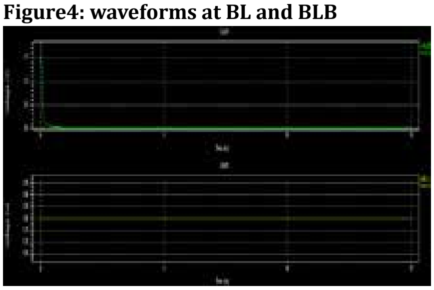
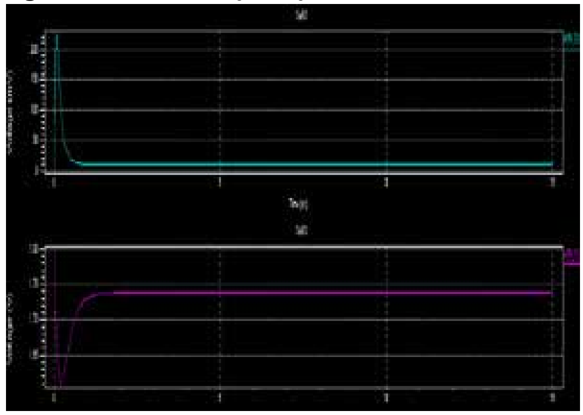
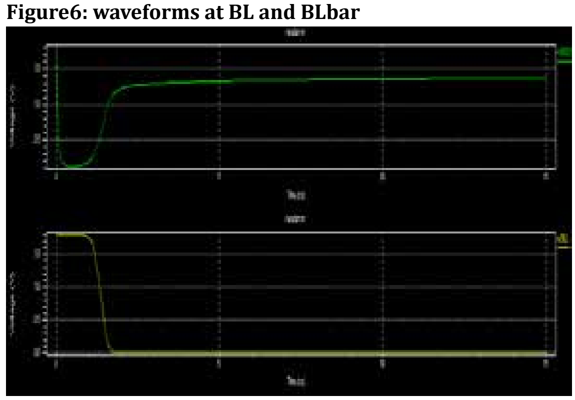


Figure5: waveforms at Q and Qbar



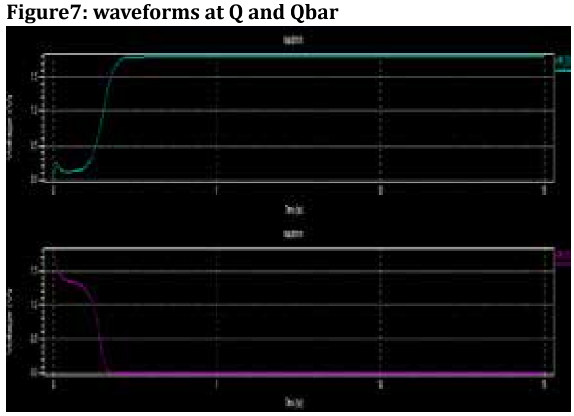
These waveforms show that data does not get flipped. So, we go on increasing the voltage till data gets flipped. The voltage at which data is flipped is 0.5V so SNM will be 0.49V, this is the maximum noise voltage that can be applied at the storage nodes without flipping the stored data. Figure6 and figure7 shows the status of BL and BLbar and Q and Qbar when data is flipped at 0.5V.

Figure6: waveforms at BL and BLbar



See the BLB line it was initially precharged to Vdd and during read operation it has not reached zero but has retained logic high while bitline reaches to logic zero showing the inversion condition of the stored data.

Figure7: waveforms at Q and Qbar



Average power consumed -> 1.874841e-005 watts.

B) Write Operation:

In order to calculate write SNM we suppose that the cell is storing logic 1 initially and we want to write logic 0. The initial conditions are-

.IC V(Q) = 1.8

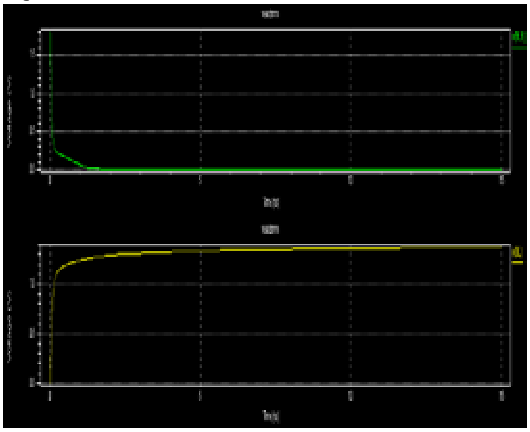
.IC V(QB) = 0

.IC V(BL) = 0

.IC V(BLB) = 1.8

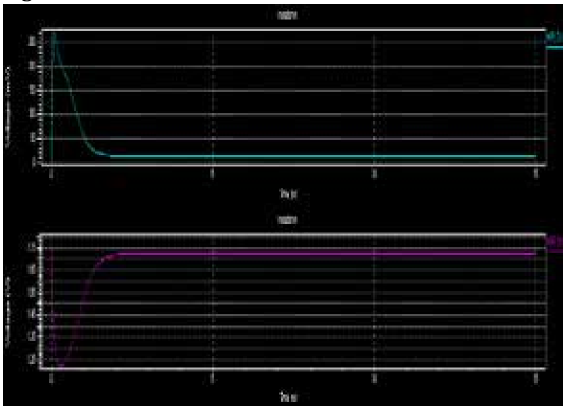
Word line signal is made high in order to carry out write operation on the 6T SRAM cell. The noise voltage is increased till the stored data flips. The following waveforms are obtained when noise voltage is 0.41V.

Figure8: waveforms at 0.41V



Here V(N_1) still remains at logic 1 and V(N_3) remains at logic 0 so data is not written successfully and we need to increase the noise voltage till the stored data flips.

Figure9: waveforms at n_1 and n_3



As we kept on increasing the voltage till 0.42V, a successful write operation takes place and data gets flipped (figure9).

Figure10: waveforms at BL and BLB

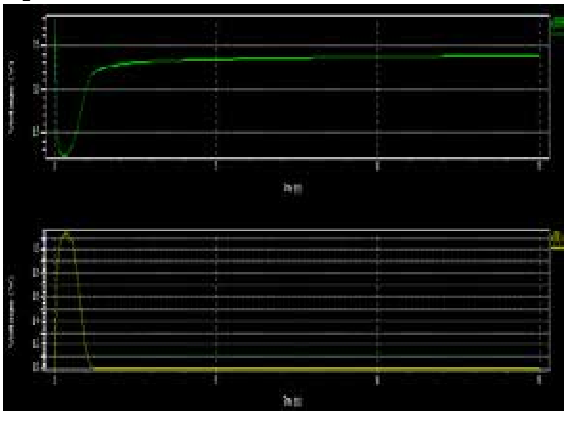
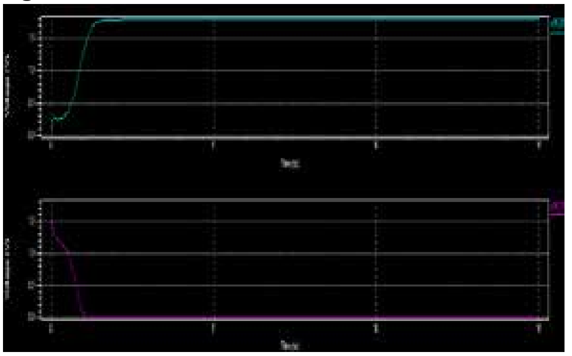


Figure11: waveforms at n_1 and n_3



It is clearly seen in the above graph that the voltage on V(N_1) has become 0 and that on V(N_3) has raised to logic high (figure11) and so data is successfully written the SRAM cell. So, write SNM is 0.41V.

Table1: Comparison of RSNM & WSNM

Read SNM	0.49 V
Write SNM	0.41V

IV. AVERAGE READ POWER CONSUMPTION

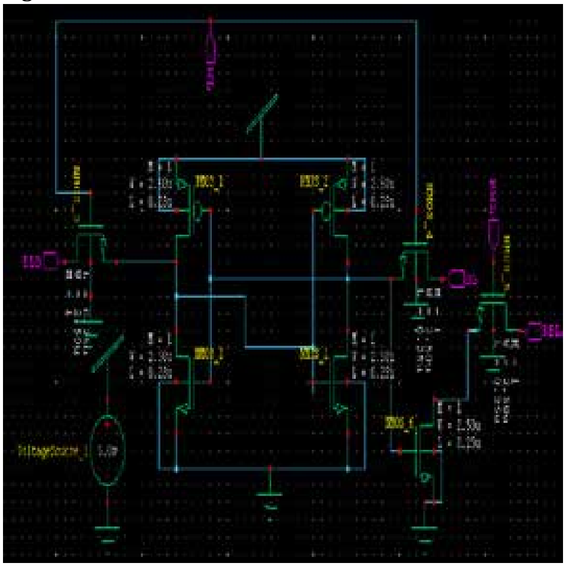
In this section, read power consumption of various SRAM cells, viz 6T, 8T, 9T and 10T would be compared.

A) 8T SRAM Cell:

To improve the stability of 6T SRAM cell has been changed and revised to 8T, [3]. In this bit-cell, read and write ports are decoupled in contrast to the 6T, so that the,

1) Read-SNM problem is eliminated;
2) 6T SRAM part can be sized for better write-ability without trading-off RSNM;
3) 2T read-buffer can be sized for larger read-current independently.

Figure12: schematic of 8T

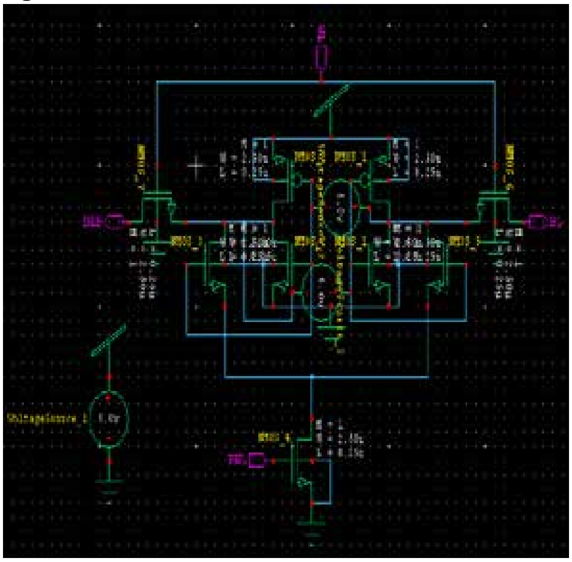


Average power consumed in case of 8T SRAM-> 6.071652e-009 watts

B) 9T SRAM Cell:

A nine transistor CMOS SRAM cell design is resented to improve the stability and therefore, the power dissipation. Separate read and write word-lines are used.

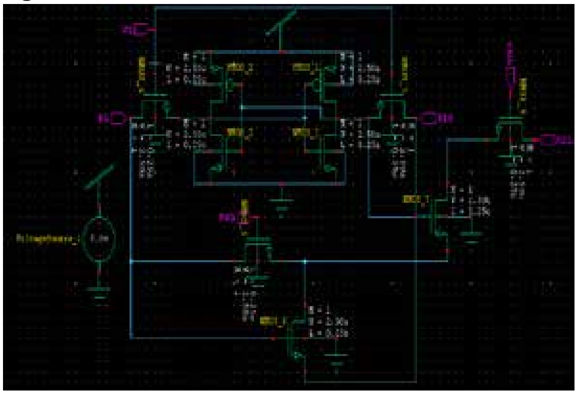
Figure13: schematic of 9T



Average power consumed: 1.943768e-005 watts

C) 10T SRAM:

Figure14. Schematic of 10T



It contains 10 Transistors, [14]. M7 and M8 constitute a separate path for read operation. M9 and M10 act as switches to conditionally connect the read path to any one of the write bit-lines depending on the last written data.

Average power consumed -> 2.430820e-009 watts

Table1.1: Comparisons of various SRAM Cells

CONFIGURATION	AVERAGE POWER CONSUMPTION
6T	1.874841e-005 watts
8T	6.071652e-009 watts
9T	1.943768e-005 watts
10T	2.430820e-009 watts

V. AREA-LAYOUT COMPARASION

A) 6T SRAM Cell:

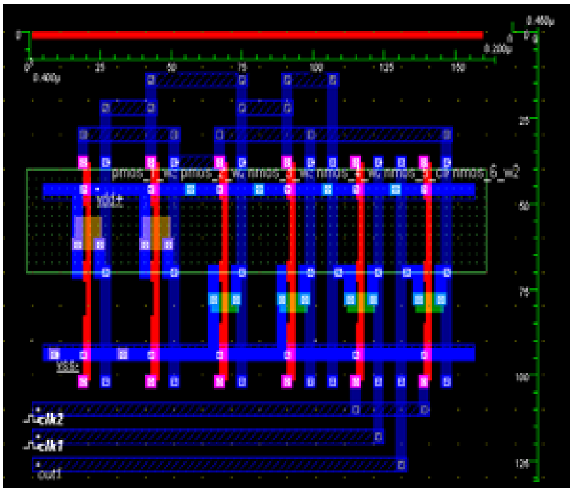


Figure15: layout of 6T

Length= 8.000u – 0.150u = 7.850u
Breadth= 6.500u – 0.650u = 5.850u
Area= l x b = 7.850 x 5.850 = 40.77um-sq

Similarly, areas of different SRAMs are calculated using microwind tool.

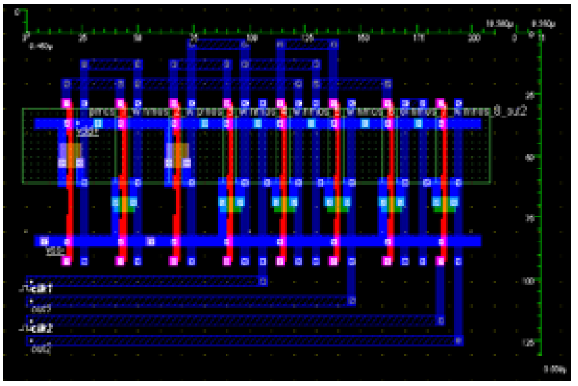


Figure16: layout of 8T

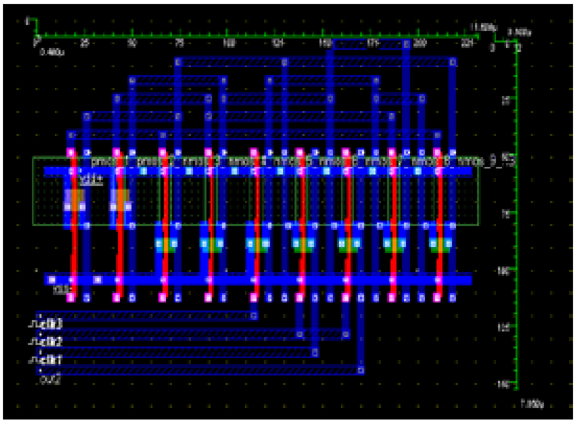
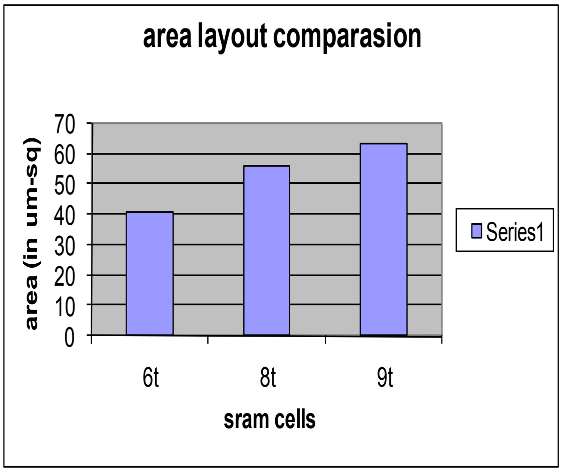


Figure17: layout of 9T



VI. CONCLUSION

The calculation for read power shows that 10T SRAM consumes the least average power during read operation. This configuration has utilized different port for reading the data and has eliminated the problem of flipping of the stored data during read operation and hence this configuration finds utility in video applications. The only disadvantage of this configuration is that it has large area overhead as compared to other configurations but when it comes to saving power and designing energy efficient SRAM 10T SRAM will be the first choice. The paper work also focused on calculating one of the important design metric of SRAM cell i.e. SNM (static noise margin) for 6T.

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