Research Paper

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Improved Performance in R-Sram Design

Engineering

KEYWORDS : Random Access Memory(RAM),Read Only Memory(ROM),SRAM design

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ABSTRACT

This paper proposes an SRAM memory cell which embeds ROM data for faster and simpler implementation of certain application such as DSP, math function evaluation, built in self test. On-chip tables stored as ROM can significantly improve the performance with no area penalty and power overhead. Standard 6T and 8T SRAM cells are embedded with ROM data by adding an extra wordline. Here the connectivity between wordlines(WL) and access transistors determines the ROM data. R-SRAM operates in SRAM as well as ROM mode.ROM data cannot be retrieved during SRAM mode.ROM data can retrieved after two special write steps which depends on connectivity of WLs. We show applications to illustrate how R-SRAM Design lead to improved performance

I. INTRODUCTION

CMOS devices have been scaled down for about 40 years to achieve better performance, higher speed and low power consumption[1]. Due to their high speed and low power SRAM based memories are commonly used rather than DRAM. Although technology scaling has led to integration of large number of transistors, a large on-chip read only memory(ROM) has not been a wide choice for designers due to their consumption of large amount of area. Large on-chip ROMs also impairs chip floorplan resulting in interconnect delay.

Few examples of applications where "on-chip tables" stored as read only memories can be effectively used are DSP, math function evaluation, BIST etc .In DSP, coefficients of FFT is usually stored as off chip memory leading to degradation in performance. Also evaluation of math function uses math function libraries stored in external nonvolatile memories. For such applications on chip ROM has significance as it improves performance.

This paper is organized as follows. Section II. deals with existing system. In section III , Introduces the proposed ,ROM embedded SRAM design methodology and section IV 6T R-SRAM design. In Section V, we show design considerations on the 6T R-SRAM including techniques to improve stability and yield. Section VI 8T R-SRAM Design

II. EXISTING SYSTEM

The conventional 6T SRAM bit cell layout topology is a standard in the industry because of its compact area, better tolerance to variability, and high performance .The conventional 6T SRAM cell is made up of six MOSFET as shown in fig. 1, in which fur transistors form the two cross coupled CMOS inverter (PL, PR, NL and NR). This is the place where a bit is stored either 1 or 0. The other two transistors (AXL, AXR) are called access transistor. It operates like pass transistors to control the access to SRAM cell by bit lines. The word line controls the functions of SRAM cell. If the WL is high the SRAM cell can be accessed. Otherwise SRAM cell is being isolated. In standby mode the word line WL is low, the access transistors will be off. The data stored in two crossed coupled inverter remain same. There won't be any change in its value as long as supply exits.

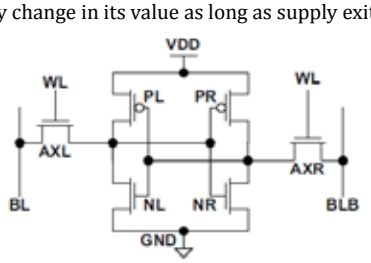


Fig 1.Conventional 6T SRAM design

During write operation data is loaded to bit line first. Then word lines are made high[3]. According to the changes in bit lines data will be stored in the two cross coupled CMOS inverter. In order to read, i.e. when data has been requested, the word line is being made high first. Before that bit lines should be precharged to VDD. As WL=1 the cell is being connected to bit lines. According to charge stored in two cross coupled inverters the bit lines will charge or discharge.

The 8T SRAM cell consists of 8 transistors. Four transistors form a cross-couple structure to store data. Two transistors act as the access transistors to the internal nodes of the cell. Access transistors connect the cell internal nodes to the BLs .

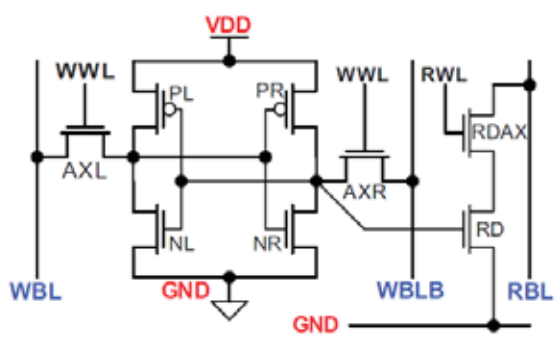


Fig2. Conventional 8T SRAM cell

Several designs have been previously proposed with this objective of embedding ROM and SRAM features. These include combining ROM and SRAM[4] in a single memory array, stacked bitline scheme based on multiple interconnect layers which allows intermixing of ROM and SRAM. This scheme increases read latency (~100%) and write power (~30%) due to resistance and capacitance of bit cells. Approaches like providing multiple power supply rails which selectively connects to SRAM cells to determine ROM data and adding extra transistors to bit cells also serves the same purpose. All the above works has significant amount of area power and performance penalty.

III. ROM EMBEDDED SRAM DESIGN

The proposed ROM Embedded SRAM (R-SRAM) design embeds ROM in SRAM. Storage cell acts as both SRAM and ROM hence no need to access external memory[8].We show 6T and 8T ROM embedded SRAM cells in this paper.

Storage cell works in two modes: SRAM and ROM

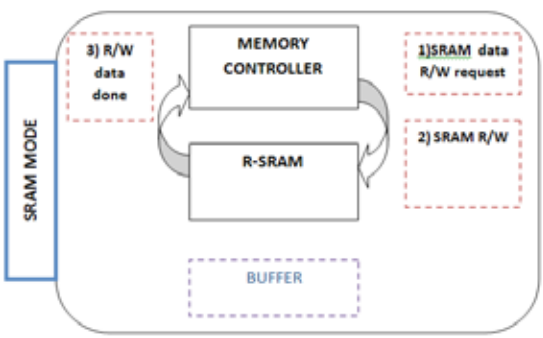
1. SRAM mode: Normal SRAM read write operation will be carried out and ROM data will not be available

2. ROM mode: When ROM data retrieval request is given SRAM data will be temporarily stored in buffer ,a two special write steps associated with connectivity of wordlines and access transistors is retrieves ROM data. After ROM data access SRAM data is transferred back to location.

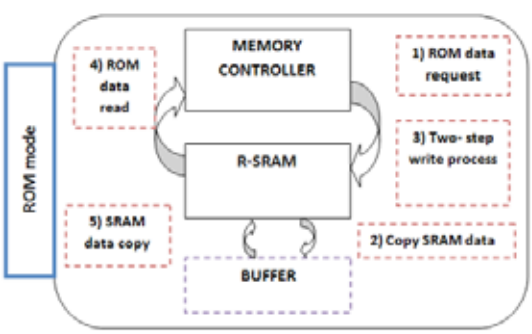
Fig 3 shows operation procedures in both SRAM and ROM mode.

IV. 6T ROM EMBEDDED SRAM DESGN

Conventional 6T SRAM cell has 2 access transistors, cross coupled inverters to store data. It has a single wordline and complementary bitlines. The cell is activated and accessed through bitlines. The schematic of conventional 6T SRAM cell is shown in Fig 2. 6T SRAM cells has an extra word line which makes it ROM embedded SRAM design. The connectivity between access transistors and WL determines the ROM data stored. Two neighboring access transistors share the same WL.



(a)



(b)

Fig 3. R-SRAM operation in (a) SRAM mode (b)ROM mode

The steps follows storing "1111" initially and in step 2 "1100" is stored in the bit cells since right access transistors of 3rd and 4th bit cells are turned off. We can retieve ROM data after the above two write steps using conventional read operation in SRAM. These two write steps of ROM data retrieval destroy the SRAM data .Hence before ROM data retrieval SRAM content is moved temporarily to a buffer of block size.

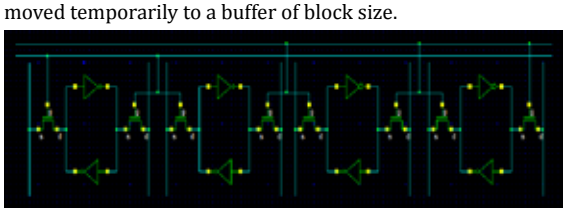


Fig 4 Schematic of 6T R-SRAM bit cell storing "1100

The height of thin cell layout of conventional SRAM cell is determined by pitch of polysilicon lines, and hence 6T R-SRAM bit cell does not incur area penalty. We have an extra routing space for additional WL.

V. DESIGN ISSUES OF 6T R-SRAM BIT CELLS

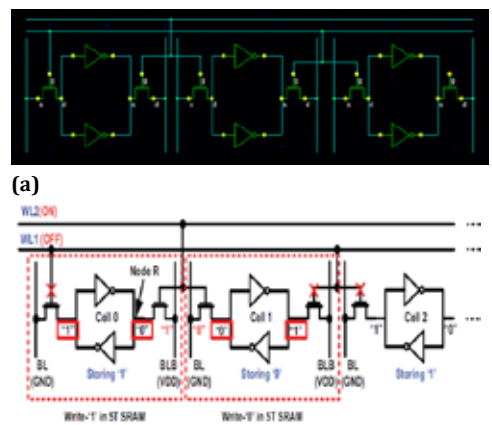
While designing the proposed 6T R-SRAM design following issues has to be considered.

1) If two consecutive bit cells have different ROM data to be embedded, step2 of R-SRAM ROM retrieving procedure performs write operation as a 5T SRAM cell, since only one access transistors is turned on. Such writing can lead to "write stability" problem in the bit cells.
2) 6T SRAM requires two WL drivers to drive separate WLs, which may lead to area/power overhead.

We analyze the above issues and propose solutions.

A)Selective Writing of Data in 6T SRAM bit cells in ROM mode:Write Stability

Write stability of 6T R-SRAM using an simple example. Fig5. shows an example of write operation(step 2 of ROM data retrieval) when three consecutive bit cells store "101"as ROM data.



(a)

(b)

Fig 5(a) Schematic of ROM operation (ROM data retrieval step 2) when ROM data s "101"(b) Circuit diagram

In Fig 5 cell 0 and cell 1 have two different connections for AXL and AXR because of two different embedded ROM data in two neighboring bit cells. First, all the bit cells are written with "111" during step 1 with the same write stability of the conventional SRAM. Then, during step 2, the content of cell 1 is written with the AXR turned off (AXR of cell 1 and AXL of cell 2 share a gate connection that is determined by the ROM data of cell 2). Cell 1 during step 2 is equivalent to a 5T SRAM bit cell (five-transistor bit cell) write "0" operation because only one access transistor (AXL) is turned on and connected to "0." Note that cell 0 has to resist being written by BLB during step 2 (BL = 0 and BLB = 1) with the AXR turned on. Cell 0 during step 2 is equivalent to the corresponding 5T SRAM bitcell write "1" operation since only one access transistor (AXR) is turned on and connected to "1." In step 2, thus, writing a "0" should occur successfully, and writing a "1" should not occur because we want only cell 1 to be written (Fig. 5). The difficulty of writing "1" through an NMOS access transistor is a well-known problem for 5T SRAMs . Interestingly, such a problem is a desirable requirement for the proposed 6T R-SRAM, as our simulations will show. Fig. 6 describes all possible access transistor connections for possible ROM data to be embedded in two consecutive neighboring 6T R-SRAM bit cells. If cell 0 and cell 1 embed ROM data "A" and "B," respectively, the connection of AXL and AXR of cell 0 to one of the two WLs is determined by "A" and "B," respectively.

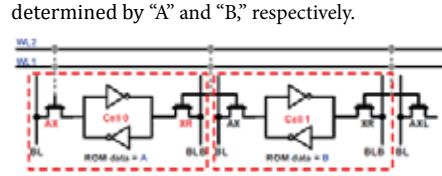


Fig6. Schematic of 2 consecutive 6T R-SRAM bit cells.

Now consider step 2 of ROM data retrieval for cell 0. The operation is equivalent to 6T SRAM bit-cell write "0" when (A = B = 0) or "hold" operation when (A = B = 1). Cell 0 equivalently performs a 5T SRAM bit-cell write "0" operation if (A = 0, B = 1) or 5T SRAM bit-cell write "1" operation if (A = 1, B = 0) during

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step 2 of ROM retrieval. For all the cases other than step 2 of ROM retrieval, 6T R-SRAM follows conventional 6T SRAM read/ write operation.

B) WL Driver Design

The proposed 6T R-SRAM requires two WL drivers to supply two WLs with the same drive strength of conventional SRAMs to maintain performance. However, additional WL drivers may lead to larger area/power overhead. Instead, the same drive strength for each WL is achieved by addition of a final-stage buffer in a single WL driver, as shown in Fig. 7 (sizes of buffers before final-stage buffers can be slightly readjusted). The drive strength of the final buffer is determined by the worst case ROM data such as all zeros or 1s (all access transistors in a row are connected to either WL1 or WL2, respectively).

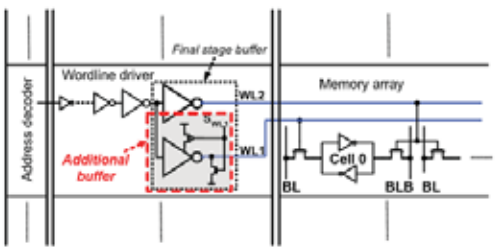
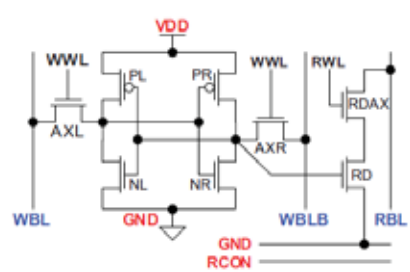


Fig7. WL driver design of 6T R-SRAM cell with additional final stage buffer.

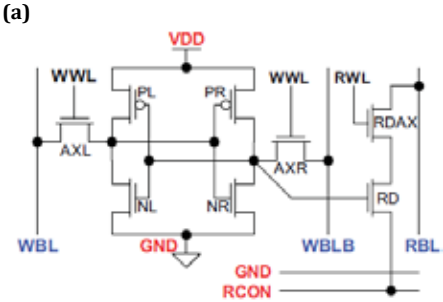
Considering the worst case, the additional buffer in 6T R-SRAM has the same size of the final-stage buffer as in conventional arrays. SWL1 in Fig. 8 controls the power supply gate of the final buffer to turn off WL1 only during step 2 in the ROM mode. The 6T SRAM array layout from a commercial memory compiler shows the WL driver taking less than 10% of the total 6T SRAM array area. The area of final stage buffers is approximately 20% of a WL driver. Hence, the area increase due to the additional buffers in our 6T R-SRAM can be less than 2% in comparison to the same size of SRAM array (readjusting the sizes of buffers before final-stage buffers has negligible impact on area increase). Our post-layout simulation results using 45-nm technology process show that additional final-stage buffers increase the power overhead by less than 1%.

VI. 8T R-SRAM DESIGN

The 8T SRAM cells isolate read and write operations using two additional transistors. The read and the write operations can be separately optimized for improved read and write stabilities, and hence the 8T SRAM is suitable for process variation tolerance and low-voltage operation in scaled technologies.



(a)



(b)

Fig 8(a) Schematic of 8T R-SRAM storing "0."(b) Schematic of 8T R-SRAM storing "1."

The schematic and layout of our 8T R-SRAM is shown in Fig8. As can be observed, 8T SRAM has two separate WLs for read and write . Since the 8T SRAM has the same height as the 6T SRAM (both bit cells are two-poly-pitch-based there is no space to introduce an additional WL to the 8T SRAM for embedding ROM features. Instead, the transistor RD of the 8T R-SRAM can be connected to either ground or to the signal ROM-control signal (RCON) (note that RD in standard 8T SRAM is always connected to ground). RCON is connected to ground during normal SRAM operations of the 8T R-SRAM. Two added transistors to the conventional 6T SRAM in thin-cell 8T SRAM layout creates enough routing space for RCON metal layer, as can be observed in Fig. 5. To perform ROM data retrieval from the 8T R-SRAM, we write "0"s to all bit cells, similar to the 6T R-SRAM. Then, all RD transistors of the 8T R-SRAM are turned on.

When we read ROM data after write "0"s, RCON is driven by the supply voltage. If RD is connected to the ground, we can read "0" through read bit line (RBL) [Fig. 5(a)]. On the other hand, if RD is connected to RCON (supply voltage), the RBL maintains the precharged voltage level, and we can read "1" [Fig. 8(b)]. Compared to the two write steps of the 6T R-SRAM (during the ROM data retrieval), the 8T R-SRAM requires only one write step. Because of the sharing, rows 1 and 2 store the same ROM data and we read either rows 1 and 2. Therefore, the ROM area density is half that of the SRAM in 8T R-SRAM. In 8T R-SRAM, RCON routing is done in every column in the vertical direction like bit lines. Note that RCON drivers can be designed in the same way as the bit-line write drivers. In other words, RCON drivers have the same design consideration, such as area and power, as that of the bit-line write drivers. Note that 8T R-SRAM maintains the same write and read failure probabilities of the standard 8T SRAM.

In Cache, ROM data is read by conventional load instruction with unique virtual address space assigned to the data. At present Processor architectures usually have lesser bits assigned to virtual address space as compared to bus width of processor. This is to enable faster and simpler address mapping. In AMD Opteron, a 64-b processor employs 48b for virtual address. Hence there is a room to employ additional bits in most significant bit(MSB) position of virtual address to indicate ROM operation. There is no need to find a matching physical address from virtual address. Also note that there is no need to generate a new instruction for ROM data retrieval.

VII. CONCLUSION

My researches have been conducted on 6T and 8T SRAM cells , by introducing concept of embedding ROM into SRAM cell .The R-SRAM for the 6T configuration uses one additional WL, and the SRAM access transistors are connected to one of the two WLs depending on the data to be stored in the ROM. For the 8T R-SRAM configuration, the cache connects the read transistor to either ground or RCON, depending on the data to be stored in the ROM. We analyzed both SRAM and ROM stability in scaled technologies and presented techniques to improve the yield.

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