Research Paper

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Power-Efficient Dual-Edge Triggered Sense-Amplifier Flip-Flop-Based Driving Circuit For Glitch-Free Nand-Based Dcdl

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KEYWORDS :

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ABSTRACT

Digitally controlled delay line (DCDL) is a digital circuit used to provide the desired delays for a circuit whose delay is controlled by a digital controlled word. Glitches are the most considerable factor that limits the use of DCDL in many applications. The glitch-free NAND-based circuit eliminates the glitches of DCDL. This circuit uses control bits that can be generated by using dual edge-triggered flip-flop. In the proposed method, power consumption of dual edge-triggered sense-amplifier flip-flop has been reduced using clock-gated sense-amplifier flip-flop.

I. Introduction

Digitally controlled delay line (DCDL) is a digital circuit whose delay is controlled by a digital control word. DCDL have many applications in recent VLSI circuits. Nowadays DCDLs are a key block in a number of applications, like all-digital PLL (ADPLL), all-digital DLL (ADDLL), microprocessors and memory circuits.

There are a wide variety of approaches for constructing the DCDL. Each of these approaches has its own advantages and drawbacks. The classical approach [2],[3] is designing a DCDL using a delay-cells chain and a MUX to select the required cell output. In these mux-based DCDLs, MUX delay increases as the number of cells increases. This will result in a tradeoff between the delay range and minimum delay() of the DCDL. A tree-based multiplexer topology can be used to reduce the large of MUX-based DCDLs[4]. But this results in an irregular structure which complicates layout design. The DCDL topology[5] uses again a delay cells chain, in which each cell is constructed by using NAND gates. This solves the tradeoff related to the MUX. But the input capacitance of the DCDL increases linearly with the number of cells which reintroduces a tradeoff between the number of cells and the minimum delay. It is possible to construct DCDL using a regular cascade of equal delay elements (DE)[6],[7],[8]. Here the multiplexer is conceptually spread among all cells. Using this approach, the minimum delay is very low and becomes independent of the number of cells and also allows a simple layout organization. The DCDL can be constructed again using a structure of cascaded delay elements in which each delay element is constructed by using three-state inverters (TINV). The DCDL[9] based on a cascade of equal delay elements, in which each delay element is constructed by using an inverter and an inverting multiplexer, allows a simple layout organization. Two drawbacks of this INVERTER + MUX topology are: firstly the different delays of the inverter and the multiplexer results in a mismatch between odd and even control-codes and secondly the large multiplexer delay.

Glitching is a common design problem in systems employing DCDLs which results in loss of data and increased power consumption due to unnecessary switching. In most of the applications, DCDLs are employed to process clock signals, therefore an operation that is glitch-free is required. An important condition to avoid glitching is designing a DCDL which have no-glitch in the presence of a delay control-code switching. This is supposed to be an issue at the DCDL-design level. Two contributions to the NAND-based DCDLs design includes: first it is shown and analyzed the glitching problem of the NAND-based DCDL and afterwards a novel glitch-free NAND-based DCDL is presented.

In many digital very large scale integration (VLSI) designs, flip-flop is one of the most power consumption components. The dual-edge triggering is an important technique to reduce the power consumption. Using dual-edge triggering, the flip-flop is capable of sampling data on both rising and falling edges of the clock so that only half the clock frequency is needed to obtain the same data throughput of single edge-triggered flip-flops. Two driving circuits using dual edge-triggered sense-amplifier flip-flop has been proposed for control-bit generation and also analyzed their power and area.

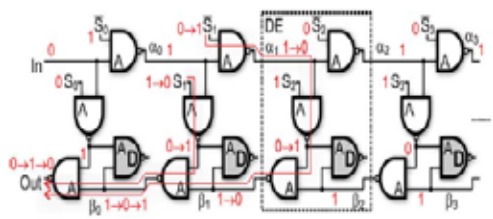

Fig.1. Glitching when the delay control-code increases by one.

II. nand-based dcdl and glitching

Fig.1. shows that the NAND based DCDL. The circuit is constructed using a series of equal delay elements (DE). Each DE is composed by four NAND gates. In the circuit "A" denotes the fast input of each NAND gate and the gates marked with "D" are dummy cells added for load balancing. The delay of the circuit is controlled through control-bit. This encode the delay control code c, such that = 0 for i < c and = 1 for i ≥ c. By using this encoding technique, each DE can be either in pass state(= 0) or in turn state (= 1). In this circuit, in fact, considering the control bits switching, it is possible to have output glitches with a stable input signal. Some examples of glitching problems of this DCDL are explained in Fig.1. Let us name S = [...] be the vector of the control-bits of the DCDL. Assuming that In = 0 and that the control-code c of the DCDL is switched from 1 (S = [0,1,1,1,...]) to 2 (S = [0,0,1,1...]). Within the structure of DCDL, the switching of and results in two different paths that will generate an output glitch. It can be easily verified that the same glitching problem exists when input *In* is 1, and the delay control-code is increased by 1 starting from an even value.

Fig. 2. shows that the DCDL structure exhibits a more complicated glitching problem when the delay control-code is increased by more than 1. Fig. 2. considers the case in which control-code c of the DCDL is switched from 1(S = [0,1,1,1,...]) to 3(S = [0,0,0,1,...]). The analysis of the figure, in this case reveals that, four paths propagate within the DCDL structure and create a multiple-glitch at the delay-line output. In DCDL applications, to avoid output glitching, the switching of delay control-bits has to be synchronized with the switching of the input signal.

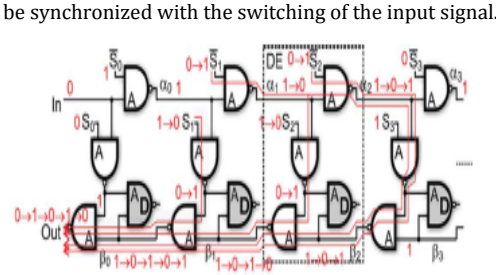

Fig. 2. Glitching when the delay control-code increases by two.

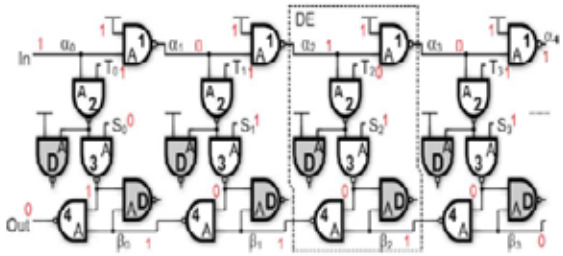

Fig 3. Glitch-free NAND-based DCDL (inverting topology)

III. glitch-free nand-based dcdl

The structure of glitch-free NAND-based DCDL is shown in Fig. 3. "A" represents the fast input of each NAND gate and gates marked with "D" represents dummy cells added for load balancing. Two sets of control-bits, and , control the DCDL and are used to synchronize the arrival of the input and the arrival of the control bits. The bits encode the control-code c, such that = 0 for i < c and = 1 for i ≥ c. The bits encode such that = 0 , = 1 for i ≠ c+1. The Fig shows the state of all signals in the case In=1and c = 1.

Each of the delay-element (DE) can be in one of three possible states, based on the chosen control-bits encoding. The DEs with i < c are supposed to be in pass-state (= 0, =1). In the pass-state the output of NAND 3 is equal to 1 and the NAND 4 allows the signal propagation in the lower NAND gates chain. The DE with i = c will be in turn-state (= =1). In the turn-state the upper input of the DE is passed to the output of NAND 3. The DE with i = c + 1 will be in post-turn-state (= 1, = 0). In the post-turn-state the output of the NAND 4 is stuck-at 1, by allowing the propagation, in the previous DE (which is in turn-state), that is, the output of NAND 3 through the gate NAND 4. All of the remaining DEs (for i > c + 1) will be constant in turn-state. The three possible states of DCDL DE and the corresponding and values are summarized in Table I.

TABLE I LOGIC-STATES OF EACH DE IN PROPOSED DCDLS

Si	Ti	DE state
0	1	Pass
1	1	Turn
1	0	Post-Turn

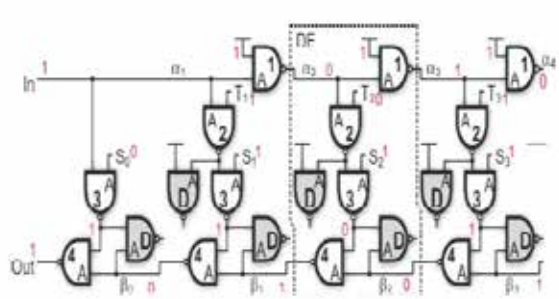

Fig. 4. Proposed glitch-free NAND-based DCDL (non-inverting topology)

A non-inverting DCDL can be constructed by modifying only the first DE, as shown in Fig. 4. The NAND gates 1 and 2 of the first DE in the circuit have been deleted, together with signal . The second DE is now having the signal equal to In, therefore the whole behavior of the DCDL is non-inverting.

IV. driving circuits for control-bit generation

For obtaining glitch-free operation of DCDL, control-bit has to be delayed with respect to control-bit . Possible driving circuits are explained in [1] and is concluded that driving circuit using clock-tree delay and dual-edge triggered flip-flop is the best.

The circuit is based on the employ of a special flip-flop, called dual-edge triggered flip-flop or double-clock flip-flop. This flip-flop make use of two different clock signals: one clock signal for capturing the high logic-state of the D input while another clock signal for capturing the low logic-state of the D input. This special flip-flop allows to control separately the LH and HL instants of switch of the signals through the delays of the two clock signals and . The clock signals delays can be implemented properly by designing the clock-tree. This solution provide low circuit complexity.

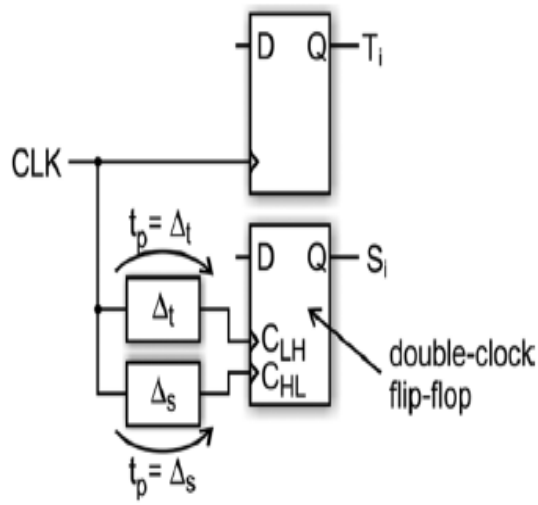

Fig. 5.delayed delays using clock-tree delay and double-clock flip-flops.

V. Proposed dual-edge triggered flip-flop

Two dual edge-triggered sense-amplifier flip-flops are discussed in [10]. The first flip-flop is dual edge-triggered sense-amplifier flip-flop (DET-SAFF) and the second one, the clock gating sense-amplifier flip-flop (CG-SAFF).

A. Dual-Edge Triggered Sense-Amplifier Flip-Flop

The circuit diagram of the proposed DET-SAFF is given. DET-SAFF is constructed using three stages: the pulse generating stage, the sensing stage and the latching stage. The dual edge-triggered pulse generator produces a brief pulse signal synchronized at both the rising and falling clock edges.

For a sense-amplifier flip-flop, in the evaluation phase, if D is low, SB will be set to high, and if D is high, RB will be set to high. Therefore, the conditional precharging technique is applied in the sensing stage, to avoid redundant transitions at major internal nodes. Two input controlled pMOS transistors, SP1 and SP2, are included in the precharge paths of nodes SB and RB, respectively. In this condition, if D remains high for n cycles, SB may only be discharged in the first cycle. For the remaining cycles, SB will be floating when PULS is low or fed to the low state DB when PULS is high. As for RB, it only requires to be precharged in the first cycle and remains at its high state for the remaining cycles. As the precharging activity is conditionally controlled, the critical pull down path of SB and RB is simplified, consisting of only one signal transistor. This helps to reduce the discharging time significantly resulting in low-power sensing stage and high-speed features.

To further improve the operating speed, a fast symmetric latch is developed which makes use of SB and RB to pull up the output nodes. The pull down path composes a PULS-controlled nMOS pass transistor, through which D (DB) is directly fed to the Q (QB) node. This topology speeds up the high-to-low output transition because the output latch immediately captures the input value once the PULS signal is generated.

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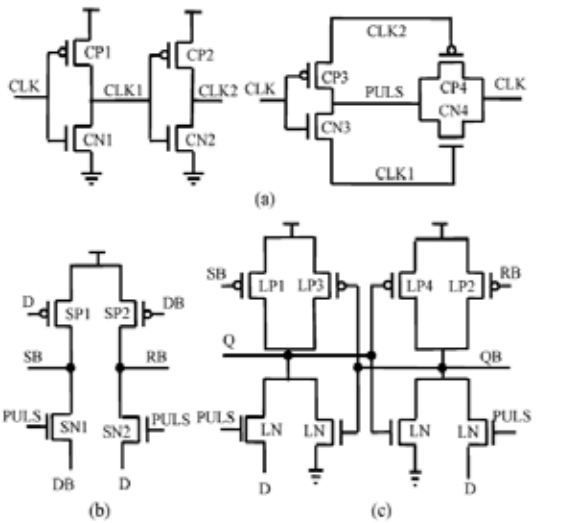

Fig. 6. Dual edge-triggered sense-amplifier flip-flop schematic: (a)dual pulse generator; (b) sensing stage; and (c) symmetric latch

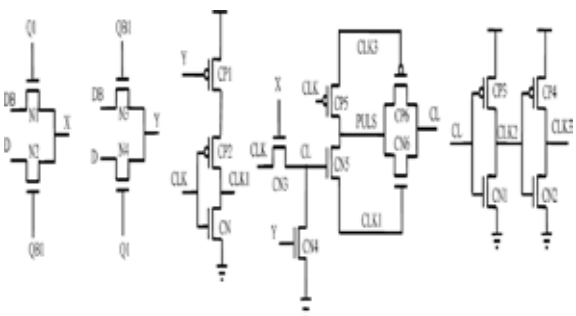

Fig. 7. Clock-gated pulse generator

B. Clock-gated Sense-Amplifier Flip-Flop

In Clock-Gated Sense-Amplifier Flip-Flop, the clock gating technique is implemented by using a control circuit in the explicit pulse generator so that the PULS signal generation is disabled in a redundant event. For comparing the previous and current input values, two comparators are included to produce signals X and Y, by using the differential inputs, D and DB, and the buffered outputs, Q1 and QB1, as control signals. If D is supposed to be different from the output Q1 (Q), X will be pulled up to high and Y to low. Transistor CN3 will be turned on to allow the clock signal to pass through as CL. CL is termed as the gated clock. At that very time, CP1 is on and drive the CLK1 signal to high before the rising edge of the clock. CL is high and its delayed signal CLK3 remains low, at the rising edge of the clock. Hence, transistor CN5 and the transmission gate are turned on, driving the PULS signal to high. After a short period of time, the transparent window is closed as CLK1 goes low and CLK3 is pulled up. Therefore, a short transparent period is created at the rising edge of the clock. The signal CLK1 is used for pulse generation rather than the signal CLK2. Such kind of design ensures that the flip-flop only captures the data at the triggering edge of the clock, thereby preventing race problems. CL is low and CLK3 is high, at the falling edge of the clock. Transistor CP5 is selected and it generates a high PULS signal. The sampling window will be shut down once CLK3 is low. When the input D remains constant in consecutive clock cycles, X is low and Y is high. CL will be pulled down by CN4 so that the corresponding CLK3 will be low regardless of the CLK signal. CLK1 may only be discharged at the first clock cycle and will maintains its low state in the remaining clock cycles. As a result, the flip-flop will remain opaque and therefore, the power can be saved.

The sensing stage is similar to DET-SAFF. Since the generated PULS signal is more heavily loaded , it does not require any clock signal and provides the most stable operation. The inner holding topology is modified to achieve buffered differential outputs, Q1 and QB1. In the clocking stage, Q1 and QB1 are used to generate X and Y instead of using Q and QB which helps to improve the performance of Clock-Gated Sense-Amplifier Flip-Flop significantly.

VI. SIMULATION RESULTS

The design of glitching and glitch-free DCDL and also its driving circuit are implemented using VHDL coding, and are synthesized and simulated using Xilinx ISE Design Suite.

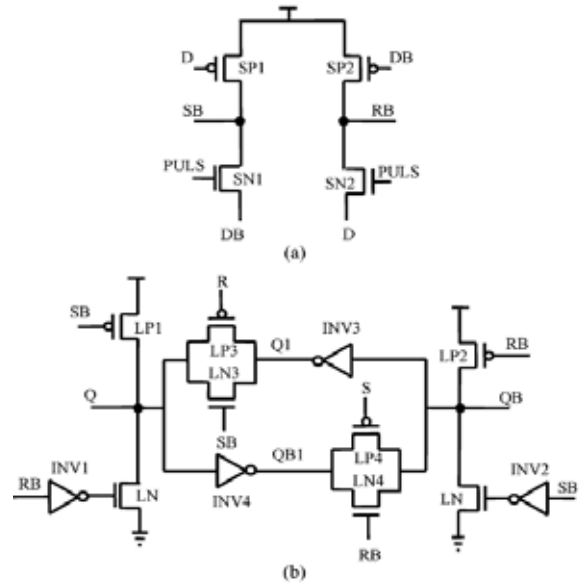

Fig. 8. Clock-Gated Sense-Amplifier Flip-Flop: (a) Sensing Stage (b) Latching Stage

A series of simulations has been performed to verify the glitching and glitch-free behavior. Dual-edge triggered sense-amplifier flip-flop based driving circuits are also implemented, synthesized and simulated in the same manner. X Power Analyzer(XPA) has been used for analyzing the power consumption of both the sense-amplifier based flip-flop and concluded that clock-gated sense-amplifier flip-flop is more power efficient than the other. Area has been analyzed in terms of total gate count used and concluded that dual edge-triggered sense-amplifier flip-flop has the lowest area.

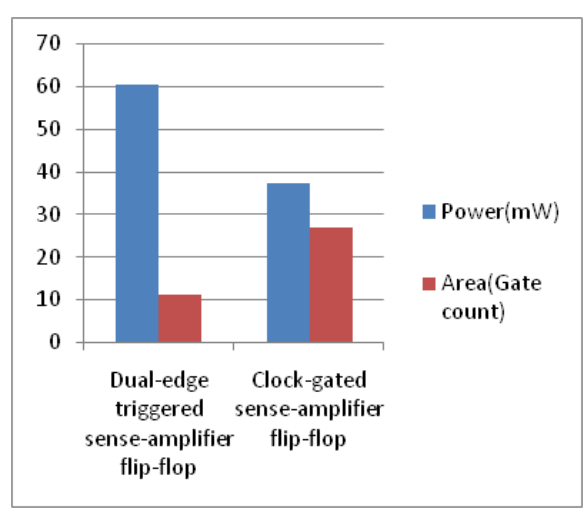

Fig. 9. Power consumption and area of dual-edge triggered sense-amplifier based flip-flops

VII. Conclusion

A Digitally Controlled Delay Lines plays an important role in many varieties of applications. Glitches are the drawback of

this DCDL which limits their employ in many applications. A NAND-based DCDL with glitching and glitch-free behavior has been presented. Control bits are used to control the Digitally Controlled Delay Line circuit and the power consumption of driving circuits are reduced by using the dual edge triggered sense- amplifier flip-flop. The simulation results confirm the correctness of NAND-based DCDL and its driving circuits.

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