



An Application of Power Reduction Using Multi Bit Flip Flop on Prbs Generator Circuit

Dhanusha A

PG Scholar, Department Of Electronics and Communication, VedaVyasa Institute Of Technology, University Of Calicut, Kerala, India

ABSTRACT

This paper presents a suitable approach for power reduction. Normally in all the systems, power consumed by clocking takes the dominant part of total power consumption . Almost all the digital systems uses the flip flops. So the power consumption of a given design can be reduced by replacing some flip flops with a multi bit flip flop. This can be implemented by using certain steps without affecting the performance of the system. In the beginning the flip flops are identified which can be merged to form a multi bit flip flop. Next all the possible combinations of flip flops to produce the multi bit flip flop is made. Next according to the combinations made, the flip flops are merged to form a multi bit flip flop. According to the experimental results, its obtained that the power is reduced by using a multi bit flip flop. The power reduction ratio can also be calculated. By using the same concept of a multi bit flip flop, the 16 bit PRBS Generator circuit is implemented and its power is compared with the power of original circuit.

Introduction

Power reduction is one of the challenges faced by the IC industry today. According to the Moore's Law, the number of transistors doubles every 18 months. So the need of power reduction is necessary. The chip area reduction also gain importance. As the technology advances the chip size get reduced and the number of components integrating in to a single chip is increasing. Low cost ,low power, small size devices are getting more attention in this world. Increase in power consumption can lead to overheating problems ,difficulty in packaging etc.[2],[3] . So power consumption has to be reduced. Several techniques has been developed to reduce the power consumption [4],[5].

The power consumed by the clock network is the dominant part of total power consumption. The clock network consumes large amount of power which accounts for half of entire chip power. So reducing clock power could reduce the power of the system.

Flip flops are the basic building blocks of all digital systems. The flip flops are used as data storage elements. They are used for storing single bit of information. A flip flop is a circuit having two stable states hence a bistable multi vibrator. Flip-flops are used in computers, communication systems , and many other types of systems. Flip-flops can be either

simple or clocked, the simple ones are commonly known as latches. The storage elements, are commonly called by word latches where as clocked devices are known as flip-flops. Level-sensitive ones are called latches, while edge-sensitive are called flip flops.

The flipflops are of different types like SR,JK, D,and T,out of which D is commonly used. The described concept is suitable for master slave D flip flops which has wide range of uses.

The clock power in such large systems having large number of flip flops can be reduced by replacing some flip flops with a multi bit flip flop. The sum of bit widths of replaceable flip flops should be the bit width of multi bit flip flop. So ,less number of flip flop means less number of clock sinks. This could reduce the power as well as area. Also the amount of routing resources can be reduced. But replacing the flip flops with a multi bit flip flop can affect the performance of the system. So to overcome that the replacement of flip flops is done in a hierarchical way without placement capacity constraint violations.

Multi Bit Flip Flops

A multi bit flip flop is made by replacing some single bit flip flops. So, the number of clock sinks will be reduced in a multi bit flip flop. Flip flops have wide range of applications. So by using multi bit flip flops the power and area can be reduced. Also more bits can be stored while comparing to single bit flip flop which can store only one bit of information. A 2-bit flip flop can

be made by merging two single bit flip flops. So when considering two single bit flip flops there will be one clock for each flip flop and in total two inverters also. But when a 2-bit flip flop is made, there will be only a single clock and inverters get reduced to one. So if a 4 bit flip flop is made, the number of inverters get reduced to 1 instead of 4 .So in multi bit flip flops the number of clock sinks get reduced and the area and power are reduced. The clock power reduction could reduce the total power. Also when many smaller flip flops are replaced with a multi bit flip flop which is larger, the reduction in device variations in the corresponding circuit occur. The number of clock sinks get reduced by reducing the number of flip flops. So the clock network formed consumes less power and thus uses less routing resources. The block diagram for two single bit flip flops before merging is shown in Fig 1.

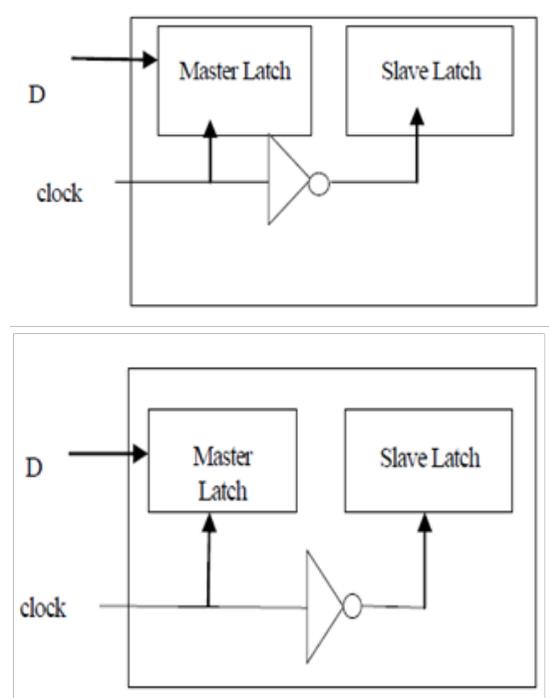


Fig.1: 2 single bit flip flops before merging

The 2 bit flip flop formed after merging is shown in Fig.2

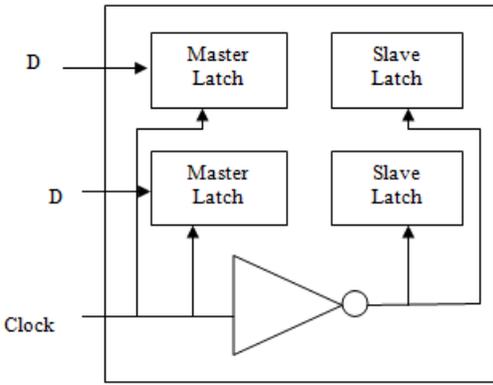


Fig. 2: 2 bit flip flop formed after merging

Proposed Method

The Flip flops are the basic unit of all digital systems. The power consumption can be reduced by reducing the clock power. The power consumed by clocks of these flip flops can be reduced in order to reduce the clock power. In this power hungry world a method to reduce power consumption is a kind of bless. The clock power is reduced by replacing some single bit flip flops with a multi bit flip flop. The replacement of flip flops with a multi bit flip flop is done in a hierarchical way. The three steps are followed for replacing the flip flops with a multi bit flip flop. The three steps for flip flop replacement used are shown in fig.3.

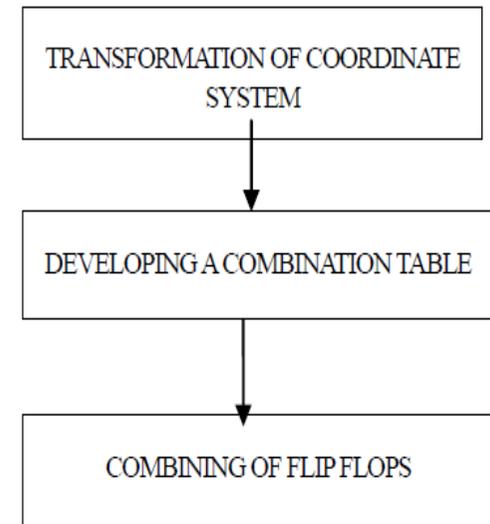


Fig.3: Steps for the proposed method

To replace the flip flops with a multi bit flip flop continuous search of flip flops to be replaced until no flip flop is left is the proper way. But with the increase in number of flip flops, it becomes a very difficult. For that these 3 steps are used.

At first, in order to recognize the flip flops to be combined, a coordinate transformation is done. Next, before combining the flip flops a combination table is developed. This gives all the possible combinations of flip flops to be combined to get the multi bit flip flop. This saves the time in finding the impossible combinations of flip flops to get the multi bit flip flop. To improve the quality and to reduce the difficulty, the whole chip region is divided into several sub regions and flip flop replacement is done in each subregion.

A. Transformation Of Coordinate System

Here, the original coordinate system of flip flop is transformed in to a new one to identify the legal placement region of each

flip flops easily. For each flip flop F, a legal placement region exists which is obtained from the overlapped areas of feasible placement regions. But, they are in diamond shape. So its very difficult to identify the overlapped area. So, its changed into rectangular shape by transforming the coordinate system of cells. The rectangular shape can be obtained by rotating the diamond shape by 45 degree.

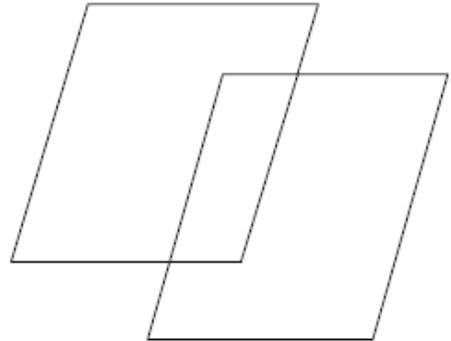


Fig. 4: Overlapped area of diamond shape

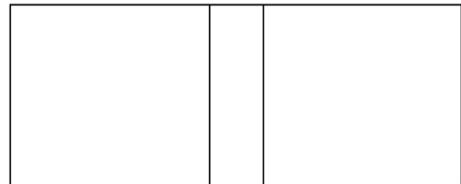


Fig.5: Overlapped area of rectangular shape
B. Developing A Combination Table

To combine several flip flops in to a new multi bit flip flop, that flip flop should be provided by the library. So a combination table is developed which records all the possible combinations of flip flops. Then the flip flops are replaced according to the order of combinations in the table. By using this the search time is reduced greatly. This can be represented as binary tree and each node represents a flip flop with a left and right leg. The sum of bit width of flip flop at right and left leg gives flip flop at the node. In order to complete binary tree certain pseudotypes are inserted. Pseudotypes are those not provided by the library.

Consider an example. Two kinds of flip flops of bit widths 1 and 4 are provided by the library. So to represent the binary tree to denote combination having bit width 4, there must be flip flops whose bit widths are 2 and 3 in library. So the pseudotypes of flip flops are inserted. Here 2 bit and 3bit flip flops are added as pseudo types. After these all combinations are sorted in ascending order. So first two combinations are selected, n1 and n2 to represent 1 bit and 4 bit flip flop respectively. Next new combinations are built. By combining two 1 bit flip flops, a 2-bit flip flop can be formed, that is combination n3. A 3 bit can be formed by combining 1 bit and 2 bit, i.e. n1 and n3 and its named as n4. Then combining n1 and n4 (1 and 3), 4 bit can be formed and its named as n5. 4 bit can be formed by combining two 2-bits also, i.e. by combining n3 and n3, new combination n6 can be formed. Among all these combinations to represent 4 bit, there are 2 combinations, n5 and n6. So to increase speed, n5 is deleted from table because its height is larger. So n4 has also been deleted. The combination table is shown in fig.6

Combination table			
n1	n2	n3	n4
1 bit	4 bit	2 bit	4 bit
		n1+n1	n3+n3

Fig.6: Combination Table

The binary tree representation is shown below.

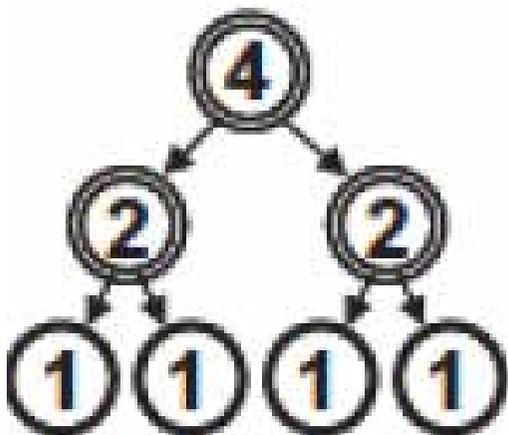


Fig.7: Binary tree representation

C. Combining Of Flip Flops

The whole chip placement region is partitioned into several sub regions. The flip flops in each sub regions are merged according to the possible combinations inserted in the combination table. The several sub regions are then combined to form the larger region. The flip flops in each subregions are merged. Then the flip flops in different subregions are merged and this is continued through whole placement region until no further flip flop is left.

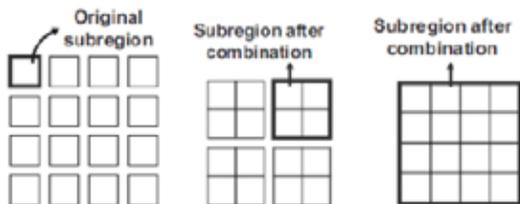


Fig.8:Combination Of Subregions in to larger ones.

iv: Experimental Results

The multi bit flip flops are formed by the three steps described above. The 2 bit flip flop ,4 bit flip flop ,8 bit flip flop and 16 bit flip flop are formed by this method .The power for all these flip flops are analyzed using Xilinx ISE 12.1i .

A. Power Comparison

The power for the multi bit flip flop and those formed by single bit flip flops are compared. They are shown in TABLE I below.

TABLE I Power Comparison

	Power consumed by single bit flip flop (W)	Power consumed by multi bit flip flop(W)
2 bit flip flop	1.88	0.52
4 bit flip flop	2.42	0.53
8 bit flip flop	3.88	0.56
16 bit flip flop	6.93	0.59

B.Graphical Representation

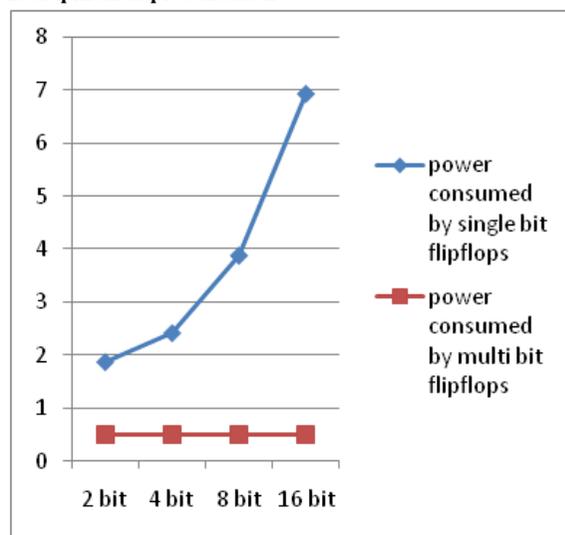


Fig.9: Graphical representation of power comparison

C. Power Reduction Ratio

The power reduction ratio can be calculated by following expression $P_RRatio(\%) = (P_original - P_merged) / P_original \cdot 100$

V.PRBS Generator

PRBS or Pseudo Random Binary Sequence is normally a random sequence of binary numbers. The PRBS Generator is random in such a way that the value of each element of the sequence is completely independent of the values of any of the other elements. It is 'pseudo' since it is deterministic. Also after N elements it starts repeating itself, comparing to real random sequence.

The implementation of PRBS generator is mainly based on the linear feedback shift register, which consists of 'n' master slave flip-flops. The PRBS generator produces a sequence of 1's and 0's which is predefined, in which 1 and 0 occurring with the same probability. LFSR is an n-bit shift register which pseudo-randomly scrolls between 2 power(n-1) values. but it does this very fast because of minimal combinational logic. Once the final state is reached, it will traverse the sequence exactly as before.

The two main parts of an LFSR is the shift register and the feedback function. A shift register is a device whose function is to shift its contents into adjacent positions within the register or, in the case of the position on the end, out of the register. The position on the other end is left empty unless some new content is shifted into the register.

In an LFSR, the bits contained in selected positions in the shift register are combined in some sort of function like XOR and the result is fed back into the register's input bit. The selected bit values are collected before the register is clocked and the result of the feedback function is inserted into the shift register during the shift operation, filling the position that is emptied after the shift.

Feedback around an LFSR's shift register comes from a selection of points called as taps in the register chain and constitutes XORing these taps to provide tap(s) back into the shift register. Here in a 16 bit PRBS generator, taps are taken as outputs of first, second, fourth and fifteenth flip flops. It is important that the output of XOR should be 1 in the beginning.

The diagram of a 16 bit PRBS Generator is shown below.

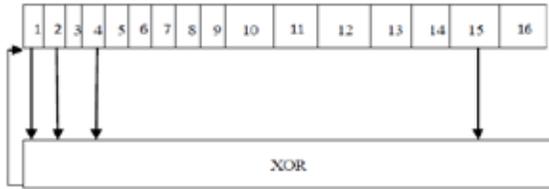


Fig.10: 16 bit PRBS Generator using single bit flip flops

In the above figure each block represents a master slave D flip flop. The same can be implemented with a single 16 bit flip flop. Then the area can be reduced. The power comparison between the 16 bit PRBS Generator using single bit flip flops and multi bit flip flops. The power comparison is shown in TABLE II.

TABLE II Power Comparison For 16 Bit PRBS Generator

Using single bit flip flops	Using 16 bit flip flop
4.474	0.574

VI.Conclusion

The power reduction is a great challenge in today’s world. In this power hungry world , this paper presents a suitable solution for power reduction in almost all digital systems.This not only reduces the power ,but also the area .The

flip flops which are the main component in all systems can be replaced with a multi bit flip flop ,in a way described in this paper. By reducing the clock sinks, the clock power can be greatly reduced. The use of multi bit flip flops reduces the routing resources. This method of replacing flip flops with multi bit flip flops doesnot affect the performance of the system.The application of this concept of multi bit flip flop was implemented in a 16 bit PRBS Generator circuit which has wide range of applications like data encryption and decryption, digital signal processing etc. in today’s world. Actually this is a bless in this power hungry world

Acknowledgment

The author greatly acknowledges the support and facilities provided by the ECE Department ,VedaVyasa Institute Of Technology under the University Of Calicut. The author also extends his acknowledgement to Mrs. Belinta Mathew, (Asst.Prof,ECE),for her immense support and help during the course of project.

REFERENCE

[1] .Ya-Ting Shyu, Jai-Ming Lin, Chun-Po Huang, Cheng-Wu Lin, Ying-Zu Lin,and Soon-Jyh Chang, "Effective And Efficient approach for power reduction using multi bit flipflops" IEEE transactions on Very Large Scale Integration (VLSI) systems, vol. 21, no. 4, april 2013. | [2]. P. Gronowski, W. J. Bowhill, R. P. Preston, M. K. Gowan, and R. L. Allmon, "High-performance microprocessor design," IEEE J. Solid-State Circuits, vol. 33, no. 5, pp. 676–686, May 1998. | [3]. W. Hou, D. Liu, and P.-H. Ho, "Automatic register banking for lowpower clock trees," in Proc. Quality Electron. Design, San Jose, CA, Mar. 2009, pp. 647–652 | [4] H. Kawagachi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% clock power reduction," in VLSI Circuits Dig. Tech. Papers Symp., Jun. 1997, pp. 97–98. | | [5]Y. Cheon, P.-H. Ho, A. B. Kahng, S. Reda, and Q. Wang. "Power-aware placement," in Proc. Design Autom. Conf., Jun. 2005, pp. 795–800 | |