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KEYWORDS :

Cordic Design For Circular and Linear Coordinate System

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ABSTRACT

In this paper we presents CORDIC circuit for circular and linear coordinate system with minimum area and power. CORDIC stands for coordinate rotation digital computer. Rotation of vectors through fixed and known angles has many applications in robotics, digital signal processing, graphics, games, and animation. We have seen the optimization schemes and CORDIC circuits for fixed and known rotations with different levels of accuracy. In this paper we are modifying the CORDIC circuit to reduce area and power if speed is not considered. We are also introducing angle mapping technique. Also instead of using simple adders we use carry select adders. CORDIC sine/cosine generators can be used in satellite data processing systems. Rotation of vectors through a fixed and known angle has wide applications in robotics, graphics, games, and animation. we use the Language, Verilog HDL in the Platform, Xilinx FPGA and Xilinx ISE 14.2 as the tool so that the proposed designs offer higher throughput, less latency and less area-delay product than the reference CORDIC design for fixed and known angles of rotation.

I. INTRODUCTION

CORDIC stands for coordinate rotation digital computer. It is described for the computation of trigonometric functions such as sin, cos, tan, sinh, cosh, tanh, multiplication, division etc. CORDIC sine/cosine generators can be used in satellite data processing systems. A vector with coordinates and angle is taken as input. vectors through a fixed and known angle has wide applications in robotics, graphics, games, and animation. Functions such as sin, cos, tan, etc appear in many problems in Signal processors, Robotics etc. so the previous computation techniques are the Taylor series and the Lookup tables. The Taylor series requires floating point. It is iterative and also slow. The Lookup tables are fast but require memory. So we use "CORDIC" so that it can save the hardware cost. It can be used when hardware Multiplier is unavailable and also when you want to save the gates required to implement. Decompose rotation operation into successive basic rotations. Each basic rotation can be realized with shift and add arithmetic operations.

The concept of CORDIC arithmetic is based on the simple and ancient principles of 2-D geometry. The iterative formulatio n of this computational algorithm was first described by Volder [1] for the computation of trigonometric functions, multiplication, division etc. A wide variety of applications of CORDIC has taken place in the area of algorithm design and development of architectures for high-performance and low-cost hardware solutions [12]. Rotation of vectors has wide applications in robotics, graphics, games, and animation [4]. Locomotion of robots is do-ne by successive rotations through small fixed angles. Interpolation of orientations between key-frames in computer graphics and animation could be done by fixed CORDIC rotations. Movement of electrons inside an atom, planets and satellites in the universe etc are the examples of uniform rotation. Another example of uniform rotation is the hands of an animated mechanical clock which perform one degree rotation each time. High-speed constant rotation is needed in games, graphic, and animation. The objects with constant rotations are used in simulation, modelling, games, animation etc.

II. OPTIMIZATION OF ELEMENTARY ANGLE SET

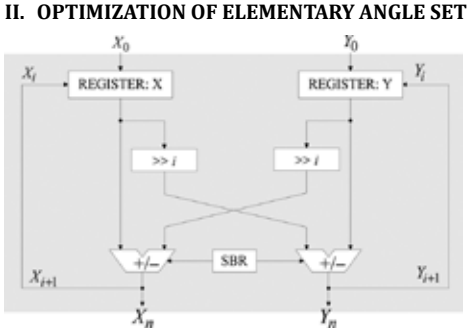

Fig. 1. Reference CORDIC circuit for fixed rotations.

and are fed as set and reset input to the pair of input registers and the successive feedback values and at the *i*th iteration are fed in parallel to the input registers. We feed the pair of input registers with the initial values and as well as the feedback values and through a pair of multiplexers.

We show here that for rotation of a vector using a rotation-mode CORDIC circuit, we can find a set of a small number of predetermined elementary angles for, 0 ≤ i ≤ m-1, where =arctan() is the elementary angle to be used for the *i*th micro-rotation and m is the minimum necessary number of micro-rotations. Meanwhile, it is well known that the rotation through any angle, between 0 to 180 degree can be mapped into a positive rotation through angle between 0 and 45 degree without any extra arithmetic operations [10]. Hence, as a first step of optimization, we perform the rotation mapping so that the rotation angle lies in the range of 0 to 45 degree .

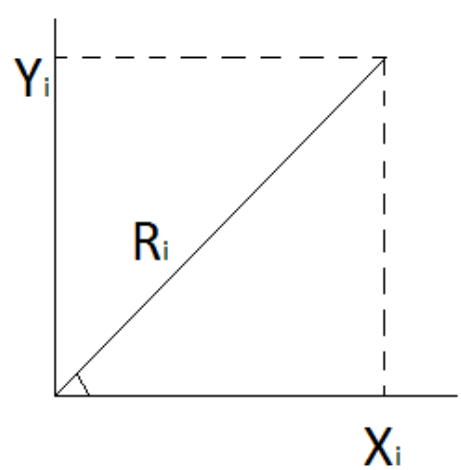

Fig. 2. Rotation of a vector (,) through an angle to (,)

III. BASIC CORDIC HARDWARE

It consists of an adder-module, two 2:1 multiplexers and a sign-bit register (SBR) of two bit size. The adder-module consist of a pair of adders/subtractors. The adders/subtractors perform additions or subtractions according to the sign-bit available from the SBR. The components of the input vector are loaded to the input-registers through set/reset input. The output of the registers are sent in two lines where the content of the register is fed to one of the adders/subtractors directly while that in the other line is loaded to the barrel-shifter pre-shifted by bit-locations to right by hardwired pre-shifting technique. The output of the adders are loaded back to the input registers for thenext CORDIC iteration.

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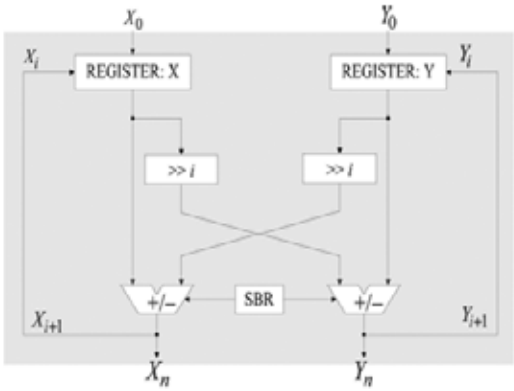

Fig. 3. Reference CORDIC circuit for fixed rotations.

The rotation-mode CORDIC algorithm to rotate a vector, U=, through an angle to obtain a rotated vector V= is given by,

$$(U_x)_{i+1} = (U_x)_i - \sigma_i.(U_y)_i.2^{-i} \quad (1)$$

$$(U_y)_{i+1} = (U_y)_i - \sigma_i.(U_x)_i.2^{-i} \quad (2)$$

$$(\emptyset)_{i+1} = (\emptyset)_i - \sigma_i.\tan^{-1}2^{-i} \quad (3)$$

such that, when n is sufficiently large

$$\begin{matrix} V_x & (U_x)_n \\ V_y = \mathrm{T}. & (U_y)_n \\ \emptyset & 0 \end{matrix}$$

The equation of the scaling factor is

$$\mathrm{T}=\prod_{i=0}^{n-1}[1+2^{-2i}]^{-\frac{1}{2}} \quad (4)$$

IV. SINE-COSINE GENERATOR

Sine-cosine generator consists of an adder-module, two 2:1 multiplexers, two right shifters and a sign-bit register (SBR) of two bit size. The adder-module consists of a pair of adders/subtractors. The adders/subtractors perform additions or subtractions according to the sign-bit available from the SBR. The components of the input vector are loaded to the input-registers through set/reset input. The output of the registers are sent in two lines where the content of the register is fed to one of the adders/subtractors directly while that in the other line is loaded to the barrel-shifter pre-shifted by bit-locations to right by hardwired pre-shifting technique. The output of the adders are loaded back to the input registers for the next CORDIC iteration. After the *n*th iteration, we get corresponding sine/cosine values.

The equations,

$$(U_x)_{i+1} = (U_x)_i - \sigma_i.(U_y)_i.2^{-i}$$

$$(U_y)_{i+1} = (U_y)_i - \sigma_i.(U_x)_i.2^{-i}$$

$$(\emptyset)_{i+1} = (\emptyset)_i - \sigma_i.\tan^{-1}2^{-i}$$

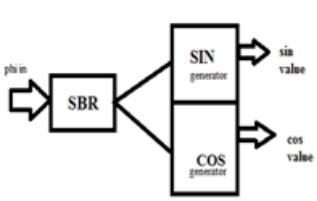

Fig. 4. Sin-cosine generator's block diagram

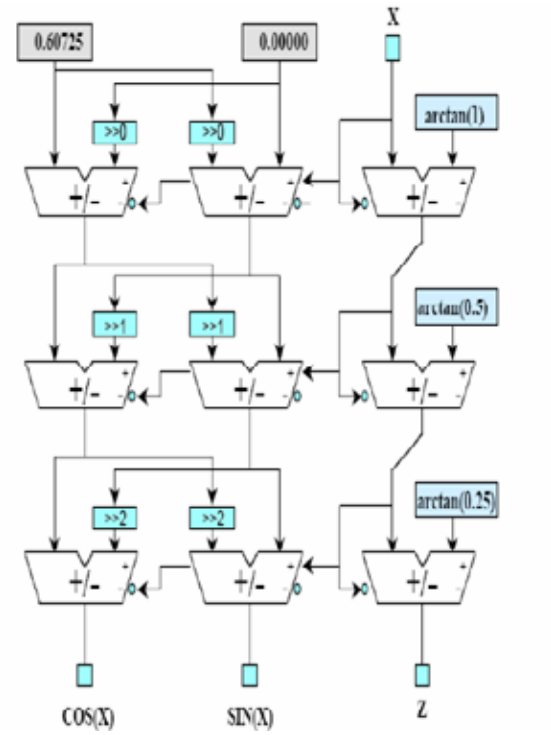

Fig. 5. Sin-cosine generator

V. BI-ROTATION CORDIC CIRCUIT

Bi-rotation cordic means, two micro-rotations. It is possible to get an accuracy up to 0.033 radian, by this technique. It can be used for some applications where the outputs are quantized, ie, in case of speech and image compression. The rotations with four and six micro-rotations can also be done by using two and three pairs of micro-rotations.

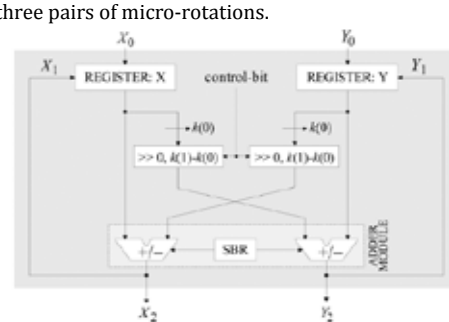

Fig. 6. Hardwired pre-shifted bi-rotation CORDIC circuit.

VI. PRE-SHIFTING

We know that, the major contributors to the hardware complexity are the barrel-shifters. A barrel-shifter for maximum of s shifts for word-length L. So if L increases, s andhardware complexity increases. If l is the minimum numberof shifts. we can load only L-l more-significant bits (MSBs) from the registers to the barrel-shifters. The barrel-shifter, therefore, needs to implement a maximum of s-l shifts only.

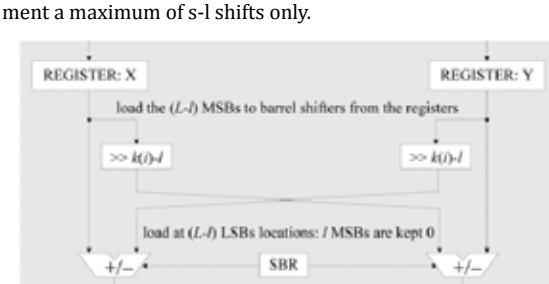

Fig. 7. Hardwired pre-shifting in basic CORDIC module.

VII. MODIFIED ARCHITECTURE OF CORDIC DESIGN TO REDUCE AREA AND POWER.

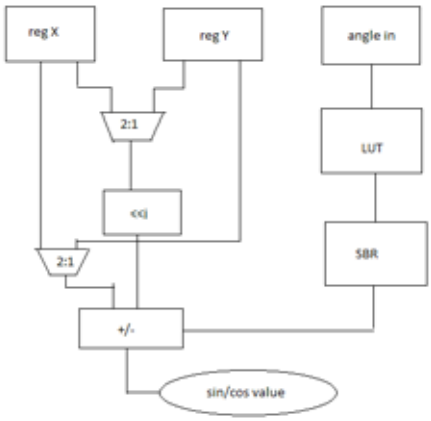

fig. 8 Proposed architecture

The above fig represents the architectural modification of the CORDIC circuit. In CORDIC circuit explained above have several number of shifters and adder/subtractors. It also have a large number of instantiations. In the above modified architecture, as compared to previous CORDIC architecture, we have less number of components. That is, we are using only have the components that used in previous CORDIC architecture. We are using only single units. we know that, the most power and area consuming component is the shifter. If we reduce the number of shifters, we can also reduce area and power consumption. If we reduce the number of components by half, then we get a 50% power reduction, by reducing the area. So we are modifying the cordic architecture inorder to reduce the power and area, if time delay is not considered. Angle mapping is an architecture to convert the input angle to a value within 0 to 45 degree. Also in the above architecture we are using a more advanced, fast, optimized adder, that is the carry select adderinorder to maximise the speed of operation.

It consists of an adder-module, two 2:1 multiplexers, a look up table, a barrel shifter and a sign-bit register (SBR) of two bit size. The adder-module consists of a pair of adders/subtractors. The adders/subtractors perform additions or subtractions according to the sign-bit available from the SBR. The components of the input vector (real and the imaginary parts of the input complex operand) are loaded to the input-registers through set/reset input. The output of the registers are fed to the 2:1 multiplexers. And its outputs are sent fed to one of the adders/subtractors directly while that in the other line is loaded to the barrel-shifter pre-shifted by bit-locations to right by hardwired pre-shifting technique. This is the architectural level modification.

VII. CONCLUSION

The conservative approximation reduces power consumption. The experimental results show that the proposed low power VLSI architecture reduces power and area by 50% compared to the conventional architecture. The throughput of the proposed architecture is comparable with the conventional architecture. The proposed CORDIC cell with interleaved scaling involves more area, but offers more throughput and involves nearly less latency and less ADP, than the reference design. The proposed single-rotation cascade and birotation cascade require, respectively, and times more area over the reference design. In this paper we are modifying the CORDIC circuit to reduce area and power if speed is not considered. we are also introducing angle mapping technique. Also instead of using simple adders we use carry select adders. CORDIC sine/cosine generators can be used in satellite data processing systems.

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