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Research Paper

Implementation of Can Bus Based System -on-Chip on Altera FPGA

Engineering

KEYWORDS : FPGA(Field Programmable Gate Array), PWM(Pulse Width Modulation),CAN (Controller Area Network).

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ABSTRACT

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing. FPGAs are going to rule in the future because of their flexibility, decreasing prices and increasingly better power efficiency. Often a soft processor is added in the FPGA design to get microcontroller like functionality along-with other concurrent processing. The Altera Stratix FPGA series is built to meet low-power, cost-sensitive design needs, enabling to get to market faster. Altera's The Nios II processor core is a soft-core central processing unit (CPU) that can be program onto an Altera field programmable gate array gives the ultimate flexibility to achieve the exact performance required for your embedded design. This project aims at implementing a CAN(Controller Area Network) Bus , NIOS soft processor core based System-on-Chip on Altera FPGA. The CAN bus module implemented inside the FPGA accepts commands from external world and passes them onto NIOS soft core in appropriate format, for it to act on the received commands. Project task includes, Porting of NIOS soft processor core onto Altera FPGA, Implementing CAN soft module inside FPGA and Programming of NIOS soft core to perform tasks based on commands received on CAN bus. Designed SOC will implement a processor task, Programmable PWM Module. This module gives out PWM waveform .The frequency and duty cycle of PWM signal would be varied based on the values received through CAN bus via Nios processor. Block coding technique in Altera QUARTUS 2 software tool is used for the complete development of System on Chip.

INTRODUCTION

Combination of large number of microcontrollers, Fpga, processors to provide control signals for controlling a product is not an efficient technique. Since it consumes large amount of power, also its size will also be uncontrollable.For controlling the set of control circuit we may require another circuit. It is not affordable and very time consuming design technique. Microcontrollers are not widely acceptable as control signal generators. Since every microcontrollers are built along with large number of peripherals .most of case the requirement of these peripherals are negligible .In many applications it would be convenient to have both a microprocessor and an FPGA array. One can have a separate RISC CPU and FPGA chips. But it is possible to combine all in one chip, leading to simpler board layout, less power consumption, and fewer problems with EMI (electromagnetic interference) and signal integrity .Soft core processors are usually used to create an FPGA-based system-on-chip (SOC).

The NIOS II is a versatile embedded processor family that presents high performance and has been created for FPGA. NIOS II Processor propitiates flexibility in the implementation of the processor system such an as Choose the exact set of CPUs,memories, interfaces needed for the application and peripherals; increase performance without changing board design, eliminate the risk of processor obsolescence; complexity, lower overall cost, and power consumption combining many functions into one chip.

The goal of this paper is to implement one of efficient system on chip on Altera PFGA. Task includes porting of NIOS II soft core processor along with peripherals according to application requirement and Implementing CAN soft module, programmable PWM module inside FPGA .After that Programming of NIOS II soft core to perform tasks based on commands received on CAN bus. Designed SOC will implement a processor task, generating Programmable PWM signal. PWM module generates signals with varying frequency and duty cycle based on values received from NIOS II system. The rest of this paper is organized as follows: Section II presents Altera Nios II Soft Processor; section IIIpresents Controller Area Network bus system; Section IV presents Design of System on chip, section V analyze simulation results ,section 6 conclusion of this work.

ALTERA NIOS II SOFT PROCESSOR

Nios II Soft Processor is a 32-bit fixed point high- performance processor created to be used in FPGA. This Softcore processor has separated buses to data and program memories, which is often called Harvard architecture, has Reduced Instruction Set Computer (RISC) architecture. Nios II system is equivalent to a microcontroller or "computer on a chip" that includes a processor and combination of peripherals and memory on a single chip. Like a microcontroller family,Nios IIsoftcore processor systems use a consistent instruction set and programming model. Altera's Nios II is a soft processor which is defined in a hardware description language can be implemented in Altera's FPGA devices by using the Quartus II CAD system. The Nios II soft processor has a number of features that can be configured by the user to meet the demands of a desired system. Its arithmetic and logic operations are performed on operands in the general purpose registers. The word length of the Nios II processor is 32 bits and all registers are 32 bits long.

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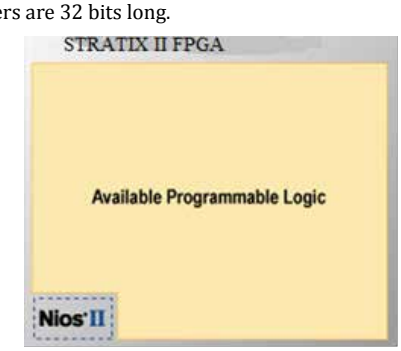

Fig 1:Cost-Effective Nios II Embedded Processor Solution

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The NIOS II processor can be implemented in three different configurations:

- Nios II/s is a "standard" version that requires less resource in an FPGA device as a trade-off for reduced performance.
- Nios II/f is a "fast" version designed for superior performance and it has the widest scope of configuration options that can be used to optimize the processor for performance.
- Nios II/e is an "economy" version which requires the least amount of FPGA resources, but also has the most limited set of user-configurable features.

CONTROLLER AREA NETWORK SYSTEM

CAN is an International Standardization Organization (ISO) defined serial communications bus originally developed for the automotive industry to replace the complex wiring harness with a two-wire bus. The CAN bus was developed by BOSCH like a multi-master message broadcast system that specifies a maximum signaling rate of 1 megabit per second (bps). CAN protocol can be defined as the set of rules for transmitting and receiving messages in a network of electronic devices. That is it defines how data is transferred from one device to another in a network.

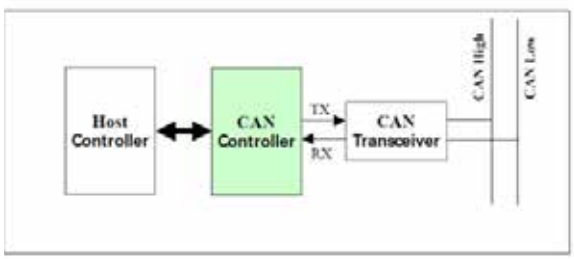

Fig 2: Connection to CAN BUS

Every node has a Host controller which is responsible for the functioning of the respective node. Along with host controller every node has a CAN controller and CAN transceiver.In this CANcontroller convert the messages of the nodes in accordance with the CAN protocols to be transmitted via CAN transceiver over the serial bus and vice versa.The CAN controller is a chip which can either be added separately or embedded inside the host controller of the node. It was designed specifically looking into the needs of the automobile industry.Now CAN's robust architecture and advantages has forced many industries like Railway, medical,Aircraftsetc to adopt CAN protocol in their systems.

DESIGN OF SYSTEM ON CHIP

Proposed system is implementing a system on chip on Altera FPGA. It includes porting a complete NIOS II system on FPGA, Porting CAN IP core onto same FPGA and generating PWM signal from programmable PWM module by NIOS II system using the duty cycle and frequency value obtained through the CAN bus system from the external world.

A .Requirement of system development

Software:

a. Altera Quartus II software Version 7.1 or later
b. Nios II Embedded Design Suite Version 7.1 or later
c. CAN IP core

Hardware:

a. Nios II Development Board

B . Block diagram of SOC

Block diagram of Proposed System shows the implementation of complete system on ALTEA FPGA. Soft cores available along with the Altera FPGA have combined together to form a system called NIOS II system using Quartus software. NIOS II System on Fpga functions like a microcontroller on Fpga. CAN IP is ported onto FPGA which works as the CAN controller for NIOS II system so that it is able to connect to external world through CAN bus. PWM module Generates Pulse Modulated Signals with varying frequency and Duty cycle according to values received from NIOS II system.

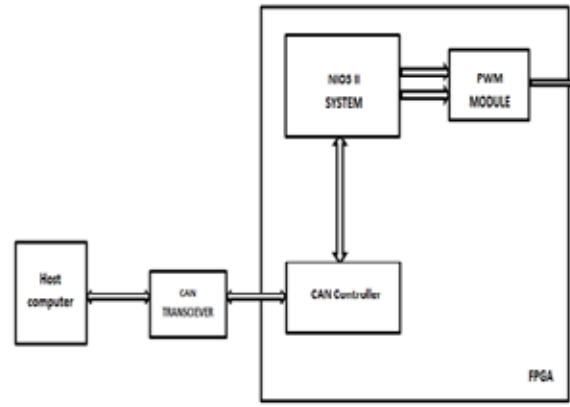

Fig 3.1: Block Diagram of final system

C. Development flow

Development flow of implementation of CAN bus based system on chip on Altera Fpga as shown in figure. First according to design specifications Nios II system have to port on to fpga. Then a programmable PWM module has to implement onto Fpga. NIOS II sytem and PWM module has to be properly interfaced.Next CAN controller IP porting on to FPGA. Which make it possible to connect the modules inside FPGA to external world. Then proper communication brtweenNios II system and CAN bus sytem also have to be made possible.

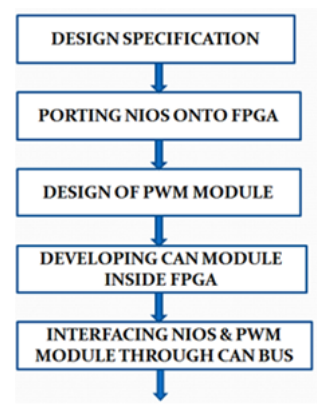

Fig 3.2 : Development Flow

D. NIOS II system

SOPC builder/ Qsys in Quartus II software allows us to design the structure of hardware system as per requirement. The Qsys generated System is shown in Figure as follows:

Fig 3.3: Qsys system

Components are interconnected by means of the interconnection network called the Avalon Switch Fabric .JTAG Debug module, is provided to allow the host computer to control the Nios II system. It makes it possible to perform operations such as downloading programs into memory, starting and stopping execution, collecting real-time execution trace data and setting

breakpoints, All parts of the Nios II system implemented on the FPGA chip are defined by using a hardware description language which is generated using Qsys Technology.

E .Programmable PWM module

Pulse width Modulation works on the principles of switching the power on and off very quickly and therefore changing the average power supplied from the source. PWM is a kind of modulation which keeps the Period of pulses constant but varying their duty cycle according to the amplitude of the modulating signal.

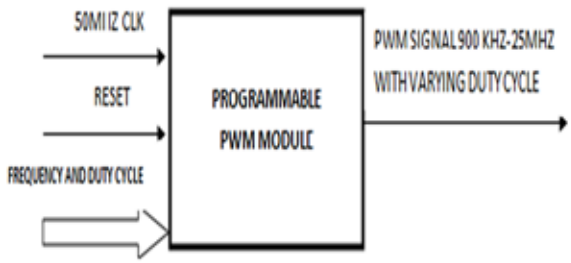

Fig3.4. 16Bit PWM module block diagram

The (ON time + OFF time) of a pulse is called 'Period' of the pulse. Duty cycle describes the proportion of 'on' time to the regular interval or 'period' of time.Duty cycle is expressed in percent, 100% being fully on. PWM has many applications such as controlling a servo motor, controlling light intensity in LEDs etc.

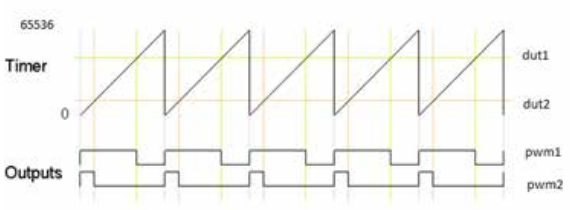

Fig3.5 PWM with varying Duty cycle.

16 bit PWM Module which is designed in such a way that it is able to generate PWM pulses with varying frequency and varying duty cycle.Counter based technique is used for the module design. Two counters are used .One is to generate varying frequency from system clock. Second is to vary the duty cycle of generated pulse. Design supports 16 bit resolution. Hence possible frequency Range 763HZ-25MHZ, Given system clock is 50 MHZ. Duty cycle can be varied up to 100%.

F .Software Details

Quartus II is a software tool produced by Altera for analysis and synthesis of HDL designs, also enables the developer to compile their designs, examine RTL diagrams,perform timing analysis, simulate a design's reaction to different stimuli and configure the target device with the programmer. The latest version is 13.1.Altera's Quartus II software provides everything need to design with Altera ® PLDs, including FPGAs, So Cs, and CPLDs. Qsys - Altera's System Integration Tool :The Qsys system integration tool saves significant time and effort in the FPGA design process by automatically generating interconnect logic to connect intellectual property (IP) functions . Qsys is the next-generation SOPC Builder tool powered by a new FPGA-optimized network-on-a-chip (NoC) technology delivering higher performance, faster verification, and improved design reuse compared to SOPC Builder. Nios II Software in Eclipse: Writing software for the Nios II processor is similar to writing software for any other microcontroller family. The Nios® Nios II software development tasks such as editing, building, and debugging to develop software for the Nios II processor.

SIMULATION RESULTS

The frequency, duty cycle values receives through CAN bus, processes the NIOS II system and transfer to PWM module. Programmable PWM module which generates the PWM signals with varying frequency and duty cycle.Simulation result is as shown in figure.

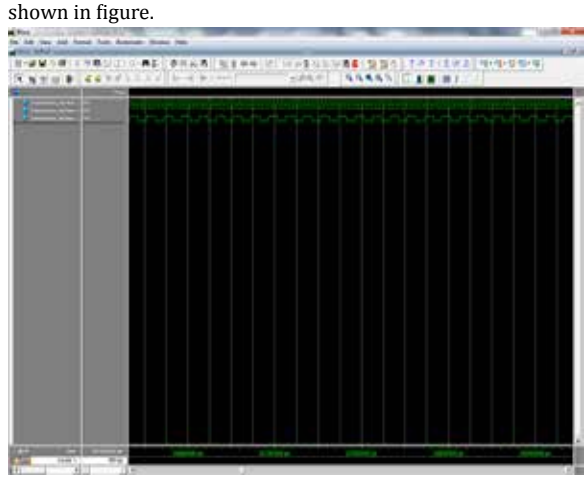

Fig 4: PWM signal simulation result

CONCLUSIONS

In this paper, We have Implemented soft Core processor such as Nios II processor based system on chip on FPGA which is dedicated only for Altera family of FPGA. The CAN bus module implemented inside the FPGA accepts commands from external world and passes them onto NIOS soft core in appropriate format, for it to act on the received commands. NIOS system is able to control programmable PWM module Implemented on same FPGA based on the values received through CAN bus. NIOS system can be Modified according to required application.

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REFERENCE

[1] First time designer guide http://www.altera.com/literature/hb/nios2/ed h_ed51001.pdf | [2]SOPCguidehttp://www.altera.com/literature/ug/ug_sopc_builder.pdf | [3]QuartusIIVersion13.0HandbookVolume4:SOPCBuilder:http://www.cs.columbia.edu/~sedwards/classes/2008/4840/qts_qii5v4.pdf | [4]AvalonInterfaceSpecifications:http://www.altera.com/mnl_avalon_spec.pdf | [5] Zuo Zhen, Tang Guilin,DongZhi,HuangZhiping,"Design ans realization of the hardware platform based on the Nios soft- core Processor" 8th International Conference on Electronic Measurement and Instruments,ICEMI 07,proc.IEEE pg 865-869,July2007 | [6]Alcalde,Ortmann,M.SMussa,S A ,"NIOS II processor Implemented in FPGA: An Application on control of a PFC Converter" Conference on Power Electronics Specialists,PESC2008.proc.IEEE pg 4446-4451,june 2008 | |