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Scl-Zsi for Interline Dvr

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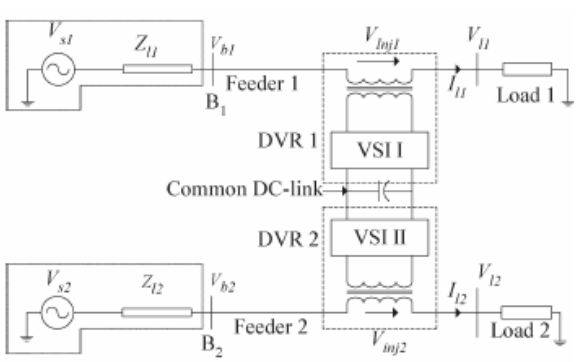
ABSTRACT

The Interline dynamic voltage restorer (DVR) is a custom power device has been proposed to mitigate voltage sags thereby protecting sensitive loads. A technique based on Embedded switched-inductor Z-source inverters have become a research hotspot because of their single-stage buck-boost inversion ability, and better immunity to EMI noises. However, their boost gains are limited because of higher component-voltage stresses and poor output power quality .To overcome these drawbacks, a new high-voltage boost impedance-source inverter called a switched-coupled-inductor quasi-Z-source inverter (SCL-qZSI) is proposed. The proposed inverter employs a unique impedance network couple with inverter main circuit and rectifier. By controlling the shoot through duty cycle, the proposed inverter system provide ride through capability during voltage sags and swells, reduces line harmonics, and improves power factor and high reliability. This paper presents the simulation results of switched-inductor Z-source inverter.

I Introduction:

Electronic devices function properly as long as the voltage (or driving force) of the supply system feeding the device stays within a consistent range. There are several types of voltage fluctuations that can cause problems, including surges and spikes, sags, harmonic distortions, and

momentary disruptions. Voltage sags are common events on the electric power network. It is one of the most severe power quality disturbances to be dealt with by the industrial sector, as it can cause severe process disruptions and result in substantial economic loss. Voltage sag is not a complete interruption of power; it is a temporary drop below 90 percent of the nominal voltage level. Most voltage sags do not go below 50 percent of the nominal voltage and they normally last from 3 to 10 cycles or 50 to 170 milliseconds. Even short duration voltage sag could cause a malfunction or a failure of a continuous process, thereby incurring heavy financial loss. The IDVR system consists of several DVRs in different feeders, sharing a common DC-link. A two-line IDVR system shown in Fig.1 employs two DVRs are connected to two different feeders where one of the DVRs compensates for voltage swell/sag produced, the other DVR in IDVR system operates in power-flow control mode. The common capacitor connected between the two feeders act as the common DC supply. It is assumed that the voltage distortion in Feeder1 would have a lesser impact on Feeder2.



Figure(1) Schematic diagram of an IDVR in a two feeder system

The upstream generation-transmission system is applied and the two feeders can be considered as two independent sources. These two voltage sources Vs1 and Vs2 are connected in series with the line impedances Z_{l1} and Z_{l2} which is in-turn connected to the buses B1 and B2 as in Fig. 1. The DVR is connected in series with the feeder and the DVRs across different feeders are connected by a common DC-link. The common DC-link indicated between the two DVRs is a large capacitor that acts as a voltage storage device. A Voltage Source Inverter (VSI) is present to invert the DC supply to AC voltage, which is injected to the transformer. The load across each feeder is connected in series to the DVR, where V_{l1} and V_{l2} are the voltages across the load.

II. Power-Flow in an IDVR System

Consider the condition when one of the DVRs in the IDVR system operates in voltage-swell/sag compensating mode while the other DVRs operate in power-flow control mode to keep the DC-link voltage at a desired level. In order to establish the power exchange between the two systems, it is assumed that DVR1 is mitigating voltage swell appearing in that line and DVR2 is controlled to provide real power to the DC-link energy storage. As line2 is operating at its normal condition, the load voltage of line2 should be equal to the load bus voltage. Hence when there is no voltage swell, the load voltage of Feeder2 is equal to the bus voltage V_{b2}. Even in swell situations, the DVR2 should be operated to meet this condition while supplying real power to the common DC-link. Hence, the locus of the V_{l2} should lie on a circle with radius equal to the desired magnitude of bus voltage V_{b2}, as shown in Fig. 3. The load voltage (V_{l2}) has an advance phase angle with respect to the supply side voltage (V_{b2}), in order to inject power to the DC-link..

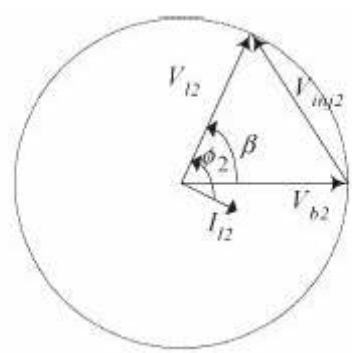


Figure (2) Vector diagram of DVR2 operating for real power exchange.

The real power exchanged between line2 and the dc-link energy storage can be written as follows:

$$P_{ex} = 3\, V_{b2}\, I_2 \cos(\Phi_2 - \beta) - 3\, V_2\, I_2 \cos\Phi_2$$

where I_2, V_{b2}, V_2, $\Phi_{2\ and}$ β are load current, load bus voltage, load voltage, load power factor (PF) angle, and load voltage advance angle of line2, respectively.

III. Modified Z-source inverter:

Fig. 4 shows the circuit of the proposed SCL-qZSI, which is obtained by replacing inductor in the classical qZSI with a com-

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bination of SC (C_3) and a three-windings (N_1 ,N_2 , and) SCL (obtained by adding winding and diode to the SC and the two-winding SCL cell in [10]). The proposed inverter consists of three diodes (D_{in} , D_1 , and D_2), three capacitors (C_1, C_2, and C_3), an input inductor L_1 , and an SCL with three windings (N_1 , N_2, andN_3). Windings N_1 and N_2 have the same number of turns (N_1- N_2), and the turn ratio of windings $N_3$to N_1 (or N_2) is n, (n=N_3/N_1=N_3/ N_2)

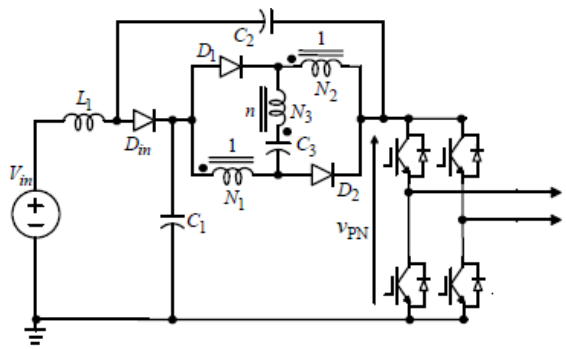


Fig. 4.Proposed switched-coupled-inductor quasi-Z-source inverter (SCL-qZSI).

The boost factor of the proposed SCL-qZSI is given by

$$B = \frac{V_{PN}}{V_{in}} = \frac{n+2}{(1-(3+n)D} (0)$$

IV. Voltage Compensation in a Two Feeder IDVR System

The voltage sag in a two-feeder IDVR system is caused due to sudden increase of the load across a feeder. Considering that the DVR1 in the IDVR system operates in voltage sag compensating mode while the DVR2 operates in power-flow control mode to keep the DC link voltage at a desired level. When there is no voltage disturbance, the load voltage of Feeder2 is equal to the bus voltage. During voltage sag, the DVR2 should be operated to meet this condition while supplying real power to the common DC link. The close loop control for both Voltage sag is illustrated.

The simulink model of the closed loop controlled IDVR for voltage sag compensation is shown in Figure (4)&(5). For a closed loop control, the output voltage across the load is rectified to give a DC voltage. This DC voltage is controlled via PI controller. The error is used and the driving pulse is generated. This pulse is fed to the converter which therefore yields in the injection of voltage. The injected voltage of the DVR depends on the accuracy and dynamic behavior of the pulse width-modulation.

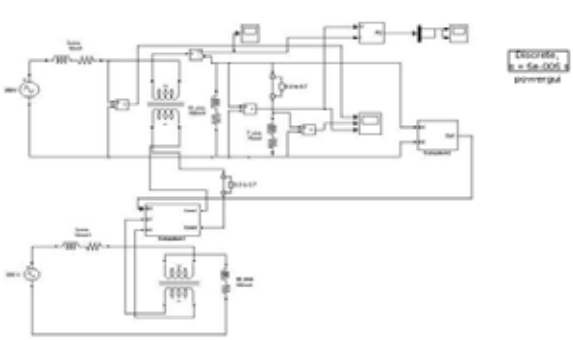
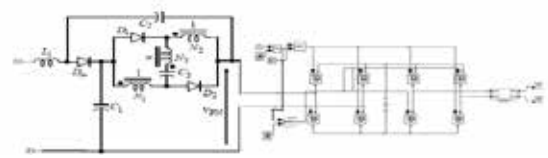


Figure (4) Closed loop control of voltage sag compensation



Figure(5) modified Zsource inverter

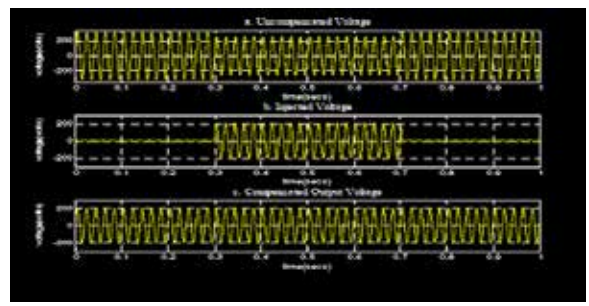


Figure (6) Simulated results of closed loop IDVR at 20% voltage sag
a. Uncompensated voltage
b. Injected voltage
c. Compensated output voltage

The Figure (6) shows the response of voltage sag compensation in a closed loop control of a two feeder IDVR system. The 260V input voltage is subjected to a sag of 20% magnitude. The voltage is injected from Feeder2 and as a result the voltage is maintained at the same value throughout the simulation, including the voltage sag. Both the real and reactive power is increased when there is an increase in the load.

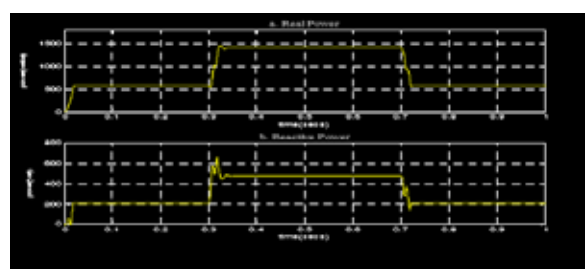


Figure (7) Real and reactive powers of feeder1 in closed loop
control of voltage sag compensation in IDVR system
a. Real power
b. Reactive power

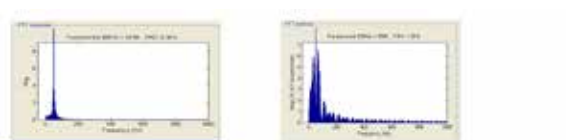


Figure (8) FFT Analysis for SCL-Z source inverter

Figure (9) FFT Analysis for conventional Z source inverter

Figure (9) shows the Total Harmonic Distortion (THD) for conventional z source inverter is 1.36%. For SCL-Z source inverter THD is reduced to 0.36%. The distortions produced in the voltage waveform for a SCL-Z source inverter is comparatively lesser than Conventional z-source inverter.

V Conclusion:

Hence the simulink model for 20% of voltage sag compensation is modeled and simulated. The respective THD values are obtained is shown.

Voltage Sag Compensation

Conventional Z source inverter=1.36%

SCL- Z source inverter=0.36%

The voltage compensation for both sag and swell can be implemented in a three phase IDVR system for various types of modulations.

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