

## A Review Paper based On high speed On-Chip VLSI Optical Interconnection Network



### Engineering

**KEYWORDS:** Integrated optoelectronic circuits, optoelectronics, optical interconnects (ICs), silicon photonics.

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### ABSTRACT

Intrachip optical interconnects (OIs) have the potential to outperform electrical wires and to ultimately solve the communication problem and obtain high-performance integrated circuits. In this paper, the International Technology Roadmap for Semiconductors (ITRS) is used as a reference to fulfill the requirements of silicon-based ICs must satisfy to successfully perform copper electrical interconnects (IEs). Interconnect has become a primary bottleneck in the integrated circuit design process. As CMOS technology is scaled, the design requirements of delay, power, bandwidth, and noise due to the on-chip interconnects have become more stringent. New design challenges are continuously emerging, such as delay uncertainty induced by process and environmental variations. It has become increasingly difficult for conventional copper interconnect to satisfy these design requirements. On-chip optical interconnect has been considered as a potential substitute for electrical interconnect.

### I. INTRODUCTION

As the continuous trend of Very Large Scale Integration (VLSI) circuits technology scaling and frequency increasing, interconnect delay becomes a significant bottleneck in system performances. This trend is a result of increased resistance of the interconnect when feature sizes enter the nano-meter era. From International Technology Roadmap for Semiconductors (ITRS) projection, interconnect delay can contribute to more than 50% of the delay when the feature size is beyond 180 nm. As a result, delay optimization techniques for interconnect are increasingly important for achieving timing closure of high performance designs.

A significant effort has recently been made to develop building blocks for on-chip optical interconnects (Ois), including light sources, waveguides, WDM (wavelength division multiplexing) components, modulators, detectors, etc. While some predictions have already been made [1], [2], there is still no clear performance specifications that optical components need to exceed in order to effectively replace electrical interconnects (EIs). We are involved in a system-level interdisciplinary project on the intrachip OIs. In the present work we use the International Technology Roadmap for Semiconductors (ITRS) predictions for the EI performance as reference point for the OI requirements. Analysis of such parameters as delay, bandwidth density and power consumption is used to obtain requirements for the individual optical interconnects components. This methodology also provides prospective for OI weaknesses and missing components.

In deep sub-micrometer VLSI technologies, interconnect plays an increasingly important role. Multiple design criteria are considered in the interconnect design process, such as delay, power, bandwidth, and noise. With technology scaling, the device dimensions and clock period continuously decrease. The delay uncertainty caused by process and environmental variations consumes a significant part of the clock period, reducing both performance and yield. It has become increasingly difficult for conventional copper based electrical interconnect to satisfy these requirements. One promising candidate to solve this problem is optical interconnect. Optical devices are widely used in the telecommunication area, and have been applied as board level interconnects. The concept of on-chip optical interconnect was first introduced by Goodman in 1984 [3]. Since electrical/optical and optical/electrical conversion is required, optical interconnect is particularly attractive for global interconnects, such as data buses and clock distribution networks, where the required signal conversions can be more easily justified. Recently, several comparisons between on-chip electrical and optical interconnects have been described [4][5]. In these papers, the

inductive effects of electrical interconnect are ignored, and highly approximate parameters characterizing the optical devices are assumed. The successful realization of on-chip optical interconnect, however, greatly depends upon the development of enhanced CMOS compatible optical devices. Without a reasonable prediction of trends in optical device development, the conclusions presented in [4][5] are less definitive. Furthermore, delay uncertainty is not addressed in these papers. In [6], an optical clock distribution network and an optical network-on-chip are presented based on heterogeneous integration techniques, which are less suitable for mass IC production. Based on a practical prediction of optical device development, a more comprehensive comparison between optical and electrical interconnects is performed in this paper for different technology nodes, considering the design criteria of delay uncertainty, latency, power dissipation, and bandwidth density. This comparison is particularly challenging since optical interconnect is a fast developing technology while electrical interconnect is relatively mature.

Enhancements in integrated circuits (IC) technology have fuelled Electronics industry. The complexity of integrated circuits (Moore's Law) and performance has been achieved through continuous inventions and revolutionary advances in the chip manufacturing process, where the circuit elements are fabricated, and these elements are appropriately connected within the circuit. Chip interconnections or interconnects, serve as global wiring, connecting circuit elements and distributing power. Interconnects are used to connect components on a VLSI chip, to connect multi-chip modules on a system board. [7] Copper-based electrical interconnects are facing many challenges which are dispersion, reflections and ringing, attenuation and its variation with frequency. The high-speed signals can be distorted due to these factors. The attenuation of high frequency signals results in a need to use high-power line-drivers, which causes thermal management issues. [7] Therefore, it is necessary to consider alternate interconnect scheme for future integrated circuits. The most novel candidate is optics based interconnects. Optical interconnect due to its high bandwidth, very less signal attenuation and cross talk, is an ideal alternative to tackle the challenges imposed by electrical interconnects for both off-chip and possibly on-chip applications.

### II. EVOLUTION OF MICROELECTRONICS SYSTEMS

Microelectronics is the art, science and technology of designing and fabricating integrated circuits with small-dimension electronic devices. [8] Over the last fifty years, a synergistic effect between solid-state physics, electrical engineering, and materials science has fueled the growth of the solid state circuits industry from infancy to become

one of the largest industries in the world. The technologies behind almost all modern electronic products, which touch every aspect of human life, from computers to communication equipments, toys, food, medical technology and the automobile industry are all based on microelectronic devices and packaging technologies.

Consequently the process of device miniaturization evolved from few micrometers today, and circuit complexity has advanced from Small-Scale Integration (SSI) in 1960s, to Medium/Large Scale Integration (MSI/LSI) in 1970s, to Very Large Scale Integration (VLSI) 1990s, and Giga-Scale Integration (GSI) in 2000s. This integration continues at a break-neck speed toward a trillion transistors per chip, Tera-Scale Integration (TSI) era, in 2020s. With the passage of time, not only digital devices and memory, but also analog/mixed-signal blocks, MEMS based sensors, biological functions are also being integrated on the same die or pack to build a complete system. In reconciling with feature size miniaturization and technology divergence, and achieving Smaller, faster, and cheaper products, there exists many unprecedented difficult technological challenges at different hierarchy levels in electronic system design process [9].

Nearly all the advances in the modern day electronic systems and devices are a direct outcome of VLSI technology.

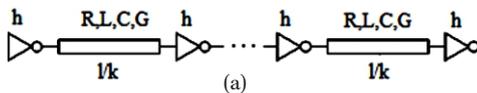
**Table 1.1 Various types of Integration Technology**

Technology	Number of gates/transistors* per chip	Examples	Year
SSI	1 to 20	74XX series, 4xxx series	60's
MSI	100 to 1000	74XXX series, 45XX series	70's
LSI	1000 to 10,000/100 to 100,000*	8085,	80's
VLSI	10,000 to 100,000/1,000,000 *	CPLD, FPGA, advanced $\mu$ C, SoC	90's

The advances in the be integration techniques can attributed directly to:-

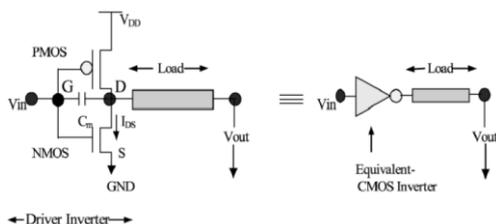
- Advances in photolithography techniques
- New designs of semiconductor devices
- Newer methods of metallization

**I. COPPER INTERCONNECT**

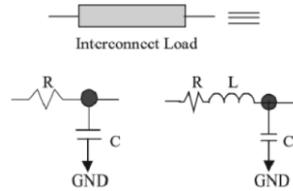


**Fig.1. Repeater insertion in an R,L,C,G interconnect.**

In copper interconnects repeater or buffer implemented as CMOS inverter [10] as shown in fig 2. A CMOS inverter is used to derive interconnect load as shown in fig 3. The CMOS inverter is the simplest buffer or repeater in VLSI interconnects. It shows a CMOS buffer driving an interconnect load and its equivalent symbolic representation. Figure 3.2 gives the equivalent RC and RLC lumped model representation of a long interconnect line. Square law models are used in which drain current changes as a square of the effective gate voltage of a long channel MOSFET, which have been used extensively for CMOS analysis.



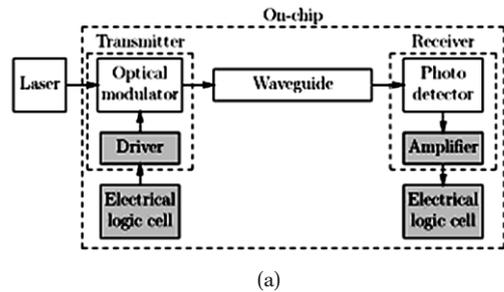
**Fig.2 CMOS buffer driving an interconnect load [10].**



**Fig.3 RLC lumped model representations of an interconnect line [10].**

**V. OPTICAL INTERCONNECT**

A promising approach to the interconnect problems is the use of an optical interconnect layer. Optical interconnection refers to the data transmission in which the data signal is transmitted as a modulation of optical carrier wave (light) through an optically transparent media such as optical fibre, planar optical waveguide or air. Optical interconnect are free from any capacitive loading effects. They do not suffer from crosstalk. The speed of propagation of a signal is determined by the speed of light and the refractive index of the optical transmission medium only. They do not suffer from electromigration- induced failure. optical interconnections operate at much higher speeds allowing the multiplexing of a large number of I/O signals. They can carry a large amount of information. Optical interconnects provide the opportunity of No pick-up of electrical noise while transmission



**Fig.4. Block diagram of an on-chip optical data path.**

The most simple optical interconnect is a point to point optical link connecting two electrical systems. It consists of a unit converting an electrical signal into an optical signal, medium to carry optical signal and a unit converting it back into electrical signal. In optical link medium is an optical waveguide which confines light along an optical transmission line. The most promising way of converting an electrical signal into light is directly modulating a light source. For high speed optical interconnect, this would be a laser. In case of many links on a chip, would require a dedicated laser per link. Integrating many small laser sources on a chip generate a significant amount of heat. So promising alternative is continuous wave light source (CW) and subsequently modulating a signal onto it. An on-chip optical link as in fig.4 contains the following components: - (a) A off chip Laser source which is coupled to the modulators; (b) Optical modulator which is used to change a property of light often of an optical beam such as a laser beam. Silicon optical modulators have been generally used. (c) an optical waveguide is used to confine light along a path on chip. Most probably a silicon strip waveguide or a rib waveguide is used for a 2-D confinement; (d) photo-detector which generates current proportional to the incoming light intensity and (e) a detector amplifier followed by gain stages.

**Transmitter**

The role of the optical transmitter is to:

- convert the electrical signal into optical form, and
- launch the resulting optical signal into the optical fiber.

The optical transmitter consists of the following components:

- optical source
- electrical pulse generator

- optical modulator

The launched power is an important design parameter, as indicates how much fiber loss can be tolerated. It is often expressed in units of dBm with 1 mW as the reference level.

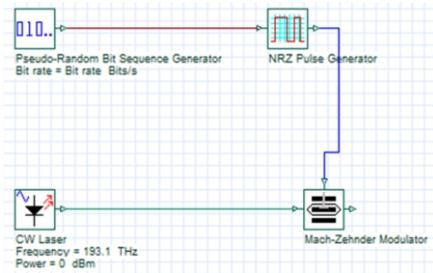


Fig.5. Component used as optical transmitter.

The transmitter in an optical interconnects system contains optical modulator, modulator driver and Electrical logical cell. LEDs and Laser Diodes are used for converting electrical signals to optical. In the circuit diagram of optical transmitter we use Pseudo-Random Bit Sequence Generator to generate bit rate in bits per second and the output of PRBSG is provided to NRZ Pulse Generator which generate the pulse provided by the PRBSG and the output of NRZ Pulse Generator is provided to Mach-Zehnder Modulator which having excitation ratio 30db. The other input of Mach-Zehnder Modulator is provided by the CW Laser which having frequency 193.1 THz and power 0dbm.

**Light sources**

The number of optoelectronic sources are available for optical interconnect. The choice of source is fundamentally based on component type (i.e VCSEL, LED, MQW modulator). In case of high speed optical interconnect, it would be a laser.

**Waveguide**

An optical waveguide is a physical structure that guides electromagnetic waves in the optical spectrum. Common types of optical waveguides include optical fiber and rectangular waveguides. Optical waveguides are used as components in integrated optical circuits or as the transmission medium in local and long haul optical communication systems.

**Optical waveguides can be classified according to their:-**

- geometry (planar, strip, or fiber waveguides),
- mode structure (single-mode, multi-mode),
- refractive index distribution (step or gradient index)
- material (glass, polymer, semiconductor).

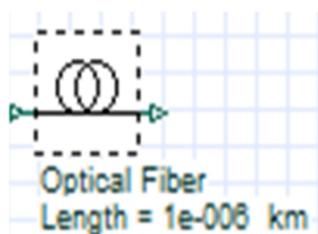


Fig.6. Component used as optical fiber.

This component is used in the circuit diagram of optical interconnect with 1cm length and wavelength of 1550nm.

Optical waveguides are the key elements of photonic devices that perform guiding, coupling, switching, splitting, multiplexing and demultiplexing of optical signals. Passive waveguides, electro optic components, transmitters, receivers, and driving electronics can be integrated into one chip using planar technology, similar to

microelectronics. Although the operation of waveguide devices is well researched and understood, their particular performance relies on many parameters—geometry, wavelength and initial field distribution, material data, and electro-optic driving conditions. These parameters must be optimized before fabricating a device. With large-scale optoelectronic circuits, accurate modeling is predominant because of the numerous resources required to fabricate a chip.

Photonic integrated circuits can combine many functions on a single chip. The most effective way for this is to use optical waveguide which confine light to propagate along a line shaped path on chip. A well known example of waveguide is an optical fiber which consists of a core with high refractive index surrounded by a lower refractive index.

**Receiver**

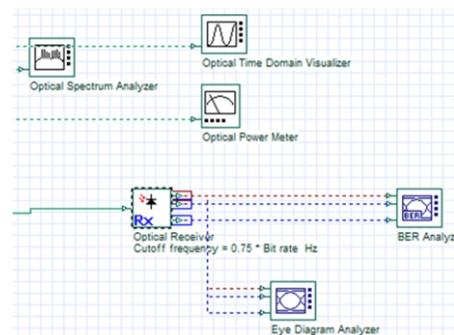


Fig.7. Component used as optical Receiver.

Optical Receiver used optical diode for receiving the optical signal and converts it into electrical signal in the circuit diagram. It uses cut off frequency  $0.75 * \text{Bit Rate}$ . For obtaining the output we use optical spectrum analyzer, optical time domain visualizer and optical power meter for optical signals For electrical signals measurement BER Analyzer and Eye Diagram Analyzer are utilized.

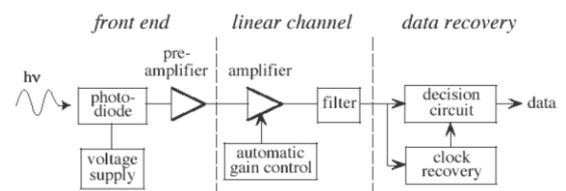


Fig.8. Block diagram of optical Receiver.

**Optical Detectors:-**

- These are transducers that convert optical signals into electrical signals.
- Transducers are devices that convert input energy of one form into output energy of another.
- An optical detector does so by generating an electrical current proportional to the intensity of the incident optical light.

**Optical detector requirements:-**

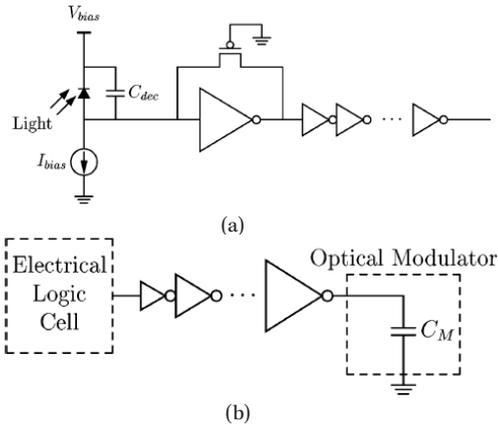
- Compatible in size to low-pass optical fibers for efficient coupling and packaging.
- High sensitivity at the operating wavelength of the source.
- Low noise contribution.
- Maintain stable operation in changing environmental conditions.

**Optical Detector Materials:-**

- Si,GaAs, GaAlAs – 850nm
- Ge, InP, InGaAs -1300nm and 1550nm.
- Materials determine the responsivity of the detector which is the

ratio of the output photocurrent to the incident optical power.

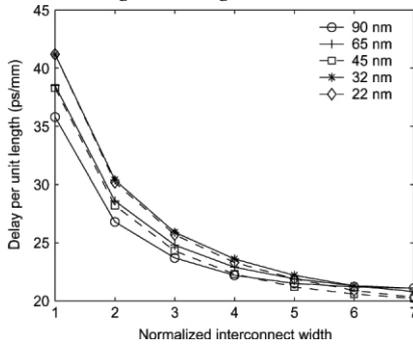
- It's a function of the wavelength and efficiency of the device.



**Fig. 9 Circuit Schematic of (a) Optical receiver and (b) Modulator driver**

At the end of the optical link the optical signals need to be converted to the electrical signal. This task is to be done by receiver. It consists of photo-detector followed by trans-impedance amplifier. Integrated photo-detector converts the incident optical power into a photocurrent. The trans-impedance amplifier performs optical-electrical conversion on the photonic interconnection layer. A variety of semiconductor photo-detectors may be used as fibre optic receivers. They are normally semiconductor devices, and a form of photodiode. A variety of diodes may be used in fibre optic receivers, namely p-n photodiode, a p-i-n photodiode, or an avalanche photodiode.

**VI Interconnect Design Challenges**



**Fig.10. Propagation delay of EI at different technology nodes versus normalized interconnects width.**

When modeling metal wire interconnects operating at multi gigahertz clock rates, it is important to consider three impedance characteristics of the wire—resistance, capacitance, and inductance. In this paper, an RLCG interconnect with equally spaced repeaters is examined for different technology nodes. Three degrees of freedom—the wire width, and the number and size of the repeaters—are explored to determine the minimum signal propagation delay. The delay model for the interconnect is an extension of work described in and includes the effects of repeater output capacitance and input signal transition time. Two of the main parameters characterizing on-chip interconnects are the propagation delay and the interconnect bandwidth density. The EI delay can be reduced by increasing the interconnect width at the expense of a smaller bandwidth density. In Fig. 10, the minimum EI delay per unit length is plotted as a function of wire width for different technology nodes. Note that technology scaling has insignificant effect on the delay of an interconnect with an optimal number of repeaters. The minimum achievable interconnect delay remains effectively fixed at approximately 20 ps/mm when technology scales from 90 nm (year 2004) to 22 nm (year 2016). Here, the maximum bit rate for a single

interconnect is assumed to be the clock rate. With this assumption, the bandwidth density increases due to the smaller wire pitch and higher clock rate. There are two major strategies for designing interconnects. Bandwidth density optimized interconnects utilize minimum sized wires but exhibit a large RC impedance. Delay optimized interconnects sacrifice bandwidth density in favor of lower delay by using wider wires. OIs are likely to initially benefit global interconnections, as EI-based global interconnects are typically delay-limited. Therefore, only delay-optimized EIs are considered for comparison with OIs. The estimated power consumption per unit length for delay-optimized EIs with optimal repeaters is of the order of 1 mW/mm and is expected to slowly increase. From this analysis, technology scaling is not expected to significantly change the EI delay; however, the EI bandwidth density is expected to increase with time. Therefore, progress in OIs must recognize that the performance of intrachip EIs is a moving (and improving) target.

**VII. Conclusion**

A detailed literature survey has been carried out and find out that the electrical interconnect in VLSI is being carried out in these days in which the present research is being carried out on the parameters like delay and power dissipation comes under. In future we consider the optical interconnect for implementing in IC's & VLSI Chip's when these are manufacturing in industry for interconnecting the transistors. In coming days both copper interconnect and optical interconnect both are the wide research areas.

**VIII. References**

- [1] Mikhail Haurylau et al., "On-Chip Optical Interconnect Roadmap: Challenges and Critical Directions," IEEE Journal of Selected Topics In Quantum Electronics, Vol. 12, No.6, November/December 2006.
- [2] Guoqing Chena, Hui Chenb, Mikhail Haurylaa, Nicholas A. Nelsona, David H. Albonesc, Philippe M. Faucheta, Eby G. Friedmana, "Predictions of CMOS compatible on-chip optical interconnect" INTEGRATION, the VLSI journal 40 (2007) 434–446.
- [3] J.W. Goodman, et al., Optical interconnects for VLSI systems, Proc. IEEE 72 (7) (1984) 850–866.
- [4] P. Kapur, K.C. Saraswat, Comparisons between electrical and optical interconnects for on-chip signaling, in: Proceedings of the IEEE International Interconnect Technology Conference, June 2002, pp. 89–91.
- [5] M.J. Kobrinsky, et al., On-chip optical interconnects, Intel Technol. J. 8 (2) (2004) 129–141.
- [6] I. O'Connor, F. Gaffiot, On-chip optical interconnect for low-power, in: E. Macii (Ed.), Ultra-Low Power Electronics and Design, Kluwer, Dordrecht, 2004.
- [7] Jaemin shin, Chung-Seok Seo, Anathasayanarn Chellappa, Martin Brooke, Abhijit Chatterjee and Nan M. Jokerst, "Comparison of Electrical and Optical Interconnect", and IEEE conference on Electronic components and technology", pp-1067-1072, 2003
- [8] Rajesh Ghongade, "VLSI Design – Introduction to the subject"
- [9] The International Technology Roadmap for Semiconductors (ITRS), 2005. [Online]. Available: <http://www.itrs.net>
- [10] Rajesh Ghongade, "VLSI Design – Introduction to the subject"