



## A REVIEW ON CONTINUOUS TIME SIGMA DELTA MODULATOR

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### ABSTRACT

This paper presents review on system level design of continuous time sigma delta modulator. A continuous time approach offers high accuracy with respect to discrete time modulator. Unity gain frequency and power can be achieved by continuous time design. as the sigma delta modulators are mainly implemented as discrete time circuits, a continuous time approach provides significant advantages for realizing high accuracy analog to digital converters at signal bandwidths where technology consideration may impose significant constraints or problems which will affect the performance of system.

### KEYWORDS:

Sigma delta modulator, Resolution, Noise Calculation, Power Calculation and Bandwidth.

### INTRODUCTION

The continuous time sigma delta modulators are affected by the non ideal behavior of analog circuit which limits their resolution in MHz bandwidth [1],[2]. The non idealities of circuit and quantization noise constitute the modulator's noise floor. The error to be reduced or noise has its own power penalty depending on the Oversampling ratio (OSR), quantize bit length (Nc), the modulator's noise shaping order (Lc), The share of each error in modulator's noise floor and OSR, Nc, Lc are the most important design parameters which will be responsible for minimizing the power consumption of a bandwidth and resolution. To get the optimum loop filter coefficients and the amplifiers specifications are the objective of given system level design approach[4]. To optimize the quantization noise, filter specifications are required and to optimize power, amplifiers specifications are required[7].

### SUMMARY

A number of research papers of various journals and conferences were studied and survey of existing literatures in the proposed area is reported and the summary of some of them are listed below:

[2] This paper presents the concept of single bit delta sigma modulators with finite impulse response feedback digital to analog converter. This modulator gives low jitter sensitivity. In a single bit design, the ADC and clock generator implementations are simple and because of that numbers of comparators are reduced; quantize gives very small power dissipation.

[4] This paper presents a automatic coefficient scaling method using an algorithm for continuous time sigma delta analog to digital converters. For high level filter specifications a short response time is required. With the utilization of a simulation method on a graphic card processor this paper provides the result in less than a minute. The GPU based synthesis tool provides the interface to enter the required design parameters and the target modulator structure and performance and desired model accuracy.

[5] This paper uses a active RC loop filter of third order and a quantize of a very low power and an excess delay compensation scheme to reduce the power dissipation. With the use of continuous time delta sigma modulator low frequency analog signals have been digitalized. This paper uses a multi-bit modulator in place of single bit modulator which provides lower in band quantization noise, lower noise due to clock jitter and lower slew rate requirements in the loop filter being used. But because of multiple feedback loops it uses more DAC which leads to larger chip area.

[6] This paper presents a fast synthesis tool which is used to design the circuit parameter of modulator. This method proved to be time efficient to design the modulator and for the systems which require long simulation times. In this paper the work shows feasibility of extending the Bandwidth range to include asymmetric digital subscriber line applications with the use of only a single supply voltage with the use of transmission gates and switched capacitor architecture. With the

proper system level design and power allocation the power dissipation could be kept low.

[7] This paper presents a new style of continuous time sigma delta modulator which is proposed by using the sigma delta modulator DAC to eliminate the error of multi-bit DAC and an FIR-DAC to improve the DAC clock jitter insensitivity. Improved stability, accuracy and reduced sensitivity to clock jitter are the advantages which are provided by multi bit sigma delta modulators. In this paper a DAC is proposed which is to be used to solve the problem of linearity in multi bit modulators while preserving their clock jitter immunity. in the outer most path a sigma delta DAC can take the place of multi-bit DAC.

### OVERVIEW

This paper provides an overview of different sigma delta and delta sigma modulator. The listed information is collected from studied paper and shown in table 1.

Ref. no.	Methodology	Result	Remark
1	Delta sigma modulators with FIR feedback ADC	SNDR- 71 dB Bw- 36 MHz Fom - 72.7 fJ/vl Supply-1.2 v	Low jitter sensitivity Highly linear
2	Automatic coefficient scaling using a genetic algorithm	Approach allows to perform between 10k and 67k simulations	Short response time
3	Using a third order active filter	Dynamic range- 93.5 dB Bw-24 MHz Supply-1.8v Power-90µw	Low power
4	Top-down design methodology	Dynamic range- 77.6 dB Power- 18.8 mw Supply-1.8v Bw-50 MHz	Switched capacitor is used
5	FIR DAC in place of multi-bit DAC	Robustness against DAC elements mismatch in the modulator	Improved stability Reduced sensitivity
6	Hybrid CT/DT sigma delta modulator	SNDR-67 dB Dynamic-rang-77dB SNR-71dB Bw-7.5 MHz	Unity gain frequency High resolution

### CONCLUSION

This paper provides an overview and analysis of (in Table I) different modulators. By applying different methods, variation in all the parameters is shown. some have less power, less response time, high linearity, stability etc. but the need for a better system level design is required which comprise of all these specifications in a single design.

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