



NATURE INSPIRED ROUTING OPTIMIZATION IN INTERCONNECTION NETWORKS

Computer Science

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ABSTRACT

The need for NoC has arisen from the developments where the number of cores in circuit has almost reached its saturation point. The effectiveness of any On Chip network depends on many factors, one of the most important being the Routing Algorithm employed. It must be designed in such a way that it can withstand faults and congestion, should be deadlock and livelock free along with proper power management. Keeping in mind the same requirements here is proposed a Nature Inspired Algorithm to address the routing problem. The algorithm was integrated into a cycle accurate full system simulator (GARNET in this case) and the results obtained were compared with pre-existing state of the art solutions. The results seem to be promising and working in lines with the standard parameters.

KEYWORDS

INTRODUCTION

The world of computation has grown exponentially in recent years, and with it, modifications on the size, power, capacity, speed, etc have also made their place in the race of improvement. This race led to different types of systems, the same goes with the On Chip Network. Network on Chip (NoC) is a new way of designing core based System on Chip which supports high degree of reusability and is scalable. A NoC can be imagined as a computer network in which computers are replaced by cores into the chip and information travels through the micro-network in the form of packets traversing on-chip links and routed by on-chip routers.

There are multiple processors, memories and other IP-blocks (Intellectual Property) which are connected to routers. The data connections between these routers are quantized into packets and transferred through this network of routers. This network facilitates effective communication between the different elements of the NoC by applying a routing scheme. Therefore there is a need for an efficient routing algorithm that can introduce a degree of modularity which would facilitate reusability and increase interoperability of these systems.

One of the major ingredients in this field of computing is Routing flits through the network of IP cores. The efficiency of the routing algorithm accounts for almost 25-30% of the system's overall performance. There are three groups of routing algorithms based on their adaptability to different traffic conditions :

- **Deterministic Routing:** Routes packets always along the same route. Most restrictive but most popular due to ease of implementation and analysis. Example: XY routing, DOR etc.
- **Oblivious Routing:** Routes packets without any information about the current network conditions as well as amount of traffic. Deterministic routing algorithms are a subset of Oblivious routing. Example: 01 Turn, Valiant routing etc.
- **Adaptive Routing:** Exploits the diversity of paths by taking routing decisions based on the current state of the network. These routing schemes can either be minimal or non-minimal.

I. Related Work

Ant Lion Optimized Bufferless Routing in the Design of Low Power Application Specific Network on Chip (Venkataraman, N. L., R. Kumar, and P. Mohamed Shakeel).

The authors here have pointed out the limitation that NoC faces when it comes to area utilization and power management as most algorithms require buffers so there is an urgent need for the development of a bufferless routing algorithm and also one which consumes less power. The proposed algorithm follows the underlying steps :

II. Initializing prioritized ant (packets) and ant lions (router path) randomly.

III. Calculate the hop count and traffic for each path.

IV. Find the most effective path

V. Update the routing table for each packet which has not reached its destination and update if the new outperforms the previous.

The results obtained are very promising when compared to any existing bufferless routing algorithm. Area utilization of planned method is $48,000 \mu m^2$, whereas FTDR and FTRD-H are $50,010 \mu m^2$ and $50,005 \mu m^2$, respectively; additionally, the operational frequency of 780.153 MHz with 0.413 mW power consumption has been achieved in this study.

Genetic algorithm for topology optimization (Ohsaki, M.)

The problem considered in this paper is to find optimal topologies with stress and displacement constraints under static loading conditions. Various algorithms have been developed for this problem. The simplest approach to topology optimization problems is the so called ground structure method. Here the necessary members are selected to form the truss of optimal topology from a highly connected ground structure with fixed nodal locations. In this paper, an algorithm based on GA is presented for topology optimization with stress and displacement constraints under multiple static loading conditions. The nodal cost as well as the member cost is incorporated in the objective function. A topological bit is introduced to define the existence of a member, and its effect on optimal topology is discussed. A global search method has been presented for topology optimization subjected to stress constraints. The singularity of the problem has been successfully overcome by using GA, which does not need sensitivity coefficients of the cost function. The nodal cost is incorporated as well as the member cost. The effect of the topological bit on the convergence of the solution is discussed. demonstrated that the use of topological bits together with the probability for existence leads to rapid convergence to the optimal topologies with a small number of members.

Proposed Routing Method

The proposed algorithm is based on the concept of genetic algorithm. The aim of the algorithm is to lower the latency and increase the throughput for given architecture and topology.

- 1) When a flit is injected into the network, its id is checked against the ids stored in the "path table". If the id is found, the corresponding path is ascribed to the flit to get to the destination.
- 2) If no data for the flit is found in the path table, then a new path is generated for the flit using a **genetic algorithm** (section 3.3.1).
- 3) Using the Genetic Algorithm process, a new path is generated and stored in the path table with its unique id.
- 4) The flit is routed across the network through the generated path.

Genetic Algorithm Modelling

Each route in the network between pairs of source and destination for the flits is modelled as a gene in the form of an integer vector, such

that for example, if there is a packet to be routed from source S to destination D, through nodes A,B and C, then a gene would be the following vector.

[S,A,B,C,D]

The set of routes for all pairs of source and destination is stored as a vector of a vector known as chromosome. Example of a possible chromosome, in case there is a packet to be routed from source S to destination D, through nodes A,B and C, and another packet is to be routed from source G to destination H, through nodes X,Y and Z, then the chromosome thus produced will be :

[[S,A,B,C,D], [G,X,Y,Z,H]]

The total population is the complete set of all chromosomes which are displayed above and look like:

[[S,A,B,C,D], [G,X,Y,Z,H]],
[[S,A,E,L,G,D], [G,X,M,H]]

The population formed here is the initial population and all the successive steps are done on the same initial population.

Initial Path Generation

Before the main algorithm starts the path is generated for the given flit by using "Hybrid XY" where X and Y direction is calculated by each router on the path on the basis of coin toss probability.

The Fitness Function

The fitness function works by taking a weighted average of congestion parameters and the maximum hop of a gene in the chromosome. The congestion parameter is calculated by checking for the common nodes occurring at the nth hop in each gene and maintaining its count. The maximum hop is the maximum length of path among the genes in a chromosome.

Tournament Selection

The selection of chromosomes for crossover is done on the basis of their fitness value. A random number 'k' is generated with values between 2 to n+1, where n is the number of genes. After this, k random chromosomes are selected from the available population and the best two chromosomes are chosen among them on the basis of their fitness value calculated as above.

Crossover

After the parent selection, a new chromosome is generated by using *uniform crossover technique*. The fitness value of this chromosome is calculated and the chromosome is added to the existing population.

Mutation

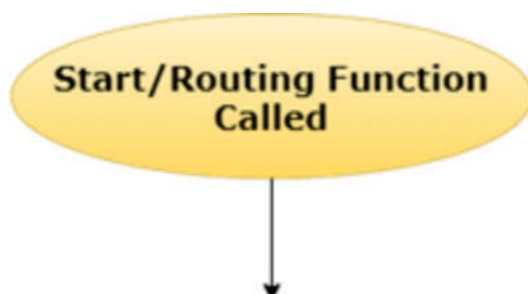
The mutation process used here is different from the traditional ones. The mutation process selects a random number of genes based on the mutation rate. The paths stored in these genes are recalculated randomly resulting in a new chromosome.

Exploitation

This is one of the most crucial and the soul of any Genetic Algorithm based solution i.e "Survival of the fittest". This is the step where the weak chromosomes i.e set of source destination path gets eliminated and the fittest among them retains its place in the population.

Routing Table

After calculating the best possible path using G.A it is stored in the routing table for future use and it remains there until the new flit is added.



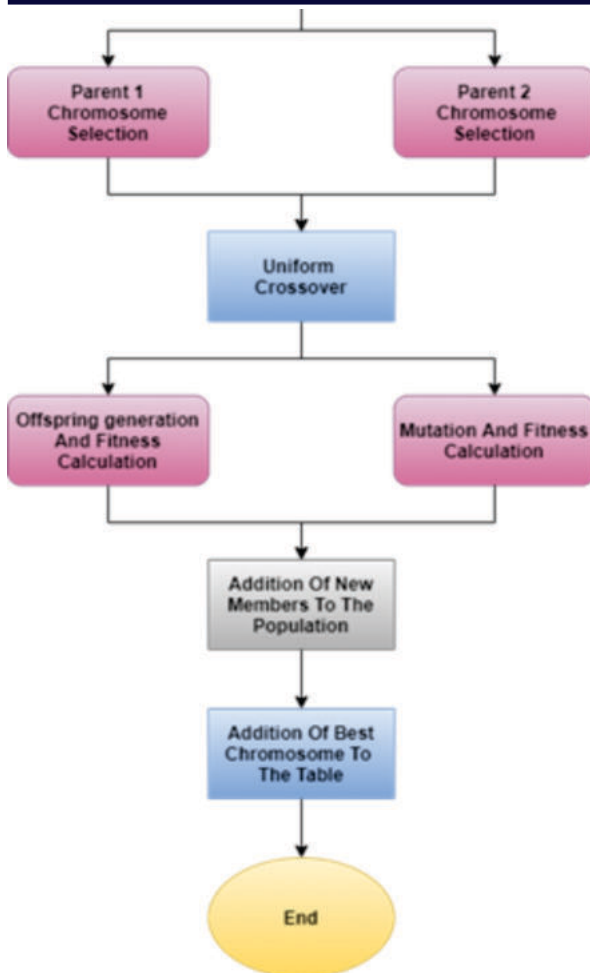


Figure 3.1 : Schematic Representation of proposed algorithm

Algorithm:

// "packet" is packet being routed; "GA_table" is routing table; "output" is the direction of next hop;

Begin

```

if packet not in GA_table then
    call Ga_apply() //function to calculate path
end if
output <- direction(packet->next_hop)

if packet at destination then //remove data of packet, if at destination
    GA_table.erase(packet)
end if

else
    remove(path_traversed) //remove already
    traversed part of the path.
end else
    return output
end
  
```

// "source destination pair" is list of source and destination of packet currently in network; "population" is the list of all "chromosomes"; "chromosome" is list of "genes"; "gene" is path from particular source to destination.

function Ga_apply()

```

do
    for each value in source destination pair do
        path <- path(source[i], destination[i])
        population.append(path)
    end for
  
```

for each chromosome in population do //calculation of fitness value for

```

each chromosome
fitness[chromosome] <- 0.75*congestion_factor + 0.25*max_hops
  
```

end for

```

for each generation do //generation of offspring and appending it to
population
chromosome1, chromosome2 <- max(chromosome_fitness)
offspring <- crossover(chromosome1, chromosome2)
    population.append(offspring)
    random_chromosome <-
random(population.chromosome)
  
```

```

replace(random(random_chromosome.gene), new(gene))
  
```

```

replace(population.chromosome, random_chromosome)
remove(worst(population.chromosome))
//removal of unfit offspring
end for
  
```

```

Ga_table.clear()
Ga_table.push(population) //adding the population to
routing table
end
  
```

function crossover()

```

do
    for each gene do
        offspring.gene <- random(chromosome1.gene, chromosome2.gene)
    end for
    return offspring
end
  
```

IV Experimental Setup and Results

Experimental Setup:

GARNET which is an NoC based model in GEM5 and is a complete cycle accurate simulator system was selected for simulation and comparison purposes. GEM5 requires a linux environment along with flex and bison.

RESULTS:

Three routing is compared and the graph is plotted for latency and throughput by noticing the flits and latency by varying injection rate. All the stats are generated by changing injection rate and keeping the below parameters constant :-

Table 4.1(a): Config Parameters

Parameters	Values
--num-cpus	64
--num-dirs	64
--network	Garnet
--topology	Mesh_XY
--mesh-rows	8
--vc-per-vnet	4
--sim-cycles	10000
--synthetic	transpose

Below are the latency values for compared algorithms with various injection rate:-

Table 4.1(b): Latency Table Values

Injection Rate	Genetic Algorithm	ROMM	XY
0.1	21.5	21.5	21.5
0.2	45	48.5	48.5
0.3	42.	41.5	41.5
0.4	71.5	75.5	82.5
0.5	91	105	125.0
0.6	213	231.5	261.5
0.7	247.5	276	306.0

Below are the throughput values obtained for the various routing algorithms compared with variable injection rate.

Table 4.1(c): Throughput table values

Injection Rate	Genetic Algorithm	ROMM	XY
0.1	0.15965732	0.15965732	0.15965732

0.2	0.15996425	0.15996425	0.15996425
0.3	0.17704280	0.17288801	0.17288801
0.4	0.19727177	0.18153200	0.18153200
0.5	0.21462829	0.20493392	0.19493392
0.6	0.21438848	0.21119424	0.20719424
0.7	0.22429906	0.21027663	0.20747663
0.8	0.22946859	0.22708314	0.22705314

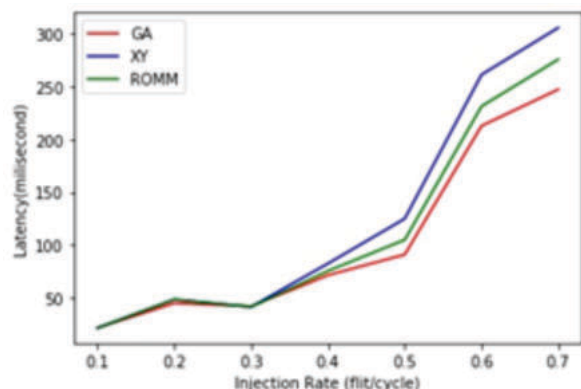


Figure 4.1(a): Latency Graph

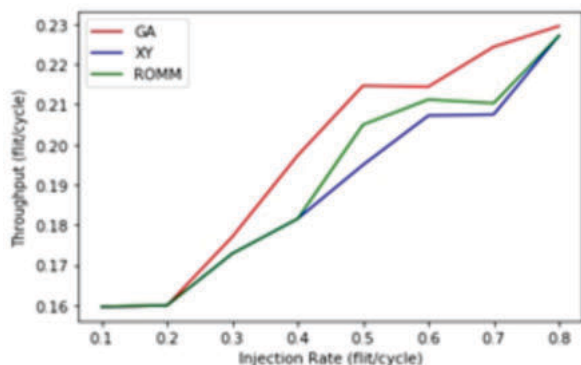


Figure 4.1(b): Throughput Graph

- The Algorithm proposed is found to be in line with the existing algorithm and significantly reduces latency and increases throughput.
- The Nature inspired algorithm has once again proved its feasibility in any type of situation with promising results.
- The simulator provides a very robust parameter and stats for the testing of the proposed solution.

CONCLUSION AND FUTURE WORK

The primary objective was to propose an algorithm for the On Chip network. The results obtained are promising. The proposed technique offers significant improvement in the throughput and latency results of the algorithm compared with XY and Random Oblivious Multidimensional Minimal Routing (ROMM). Another major parameter to consider here is the power component dimension of the performance analysis, which is an area of further improvement.

Acknowledgement:

Authors are thankful to Prof. Bansidhar Joshi for his discussions and invaluable suggestions.

REFERENCES

1. Biniha, S., and S. Siva Sathya. "A survey of bio inspired optimization algorithms." *International journal of soft computing and engineering* 2.2 (2012): 137-151.
2. Sharapov, R. R. *Genetic algorithms: Basic ideas, variants and analysis*. INTECH Open Access Publisher, 2007.
3. Braun, Heinrich. "On solving travelling salesman problems by genetic algorithms." *International Conference on Parallel Problem Solving from Nature*. Springer, Berlin, Heidelberg, 1990.
4. Hemani, Ahmed, et al. "Network on chip: An architecture for the billion transistor era." *Proceeding of the IEEE NorChip Conference*. Vol. 31. No. 20. sn, 2000.
5. Agarwal, Niket, et al. "GARNET: A detailed on-chip network model inside a full-system simulator." *2009 IEEE international symposium on performance analysis of systems and software*. IEEE, 2009.
6. Myung, Wooshik, Zhao Qi, and Ma Cheng. "Performance Analysis of Routing Algorithms in Mesh Based Network on Chip using Booksim Simulator." *2019 IEEE International Conference of Intelligent Applied Systems on Engineering (ICIASE)*. IEEE, 2019.
7. Jain, Lavina, et al. "NIRGAM: a simulator for NoC interconnect routing and application modeling." *Design, automation and test in Europe conference*. IEEE, 2007.

8. Xu, Yongfeng, Jianyang Zhou, and Shunkui Liu. "Research and analysis of routing algorithms for NoC." *2011 3rd International Conference on Computer Research and Development*. Vol. 2. IEEE, 2011.
9. Ohsaki, M. "Genetic algorithm for topology optimization of trusses." *Computers & Structures* 57.2 (1995): 219-225.
10. Jiang, Nan, et al. "A detailed and flexible cycle-accurate network-on-chip simulator." *2013 IEEE international symposium on performance analysis of systems and software (ISPASS)*. IEEE, 2013.
11. GE Fen, WU Ning. "Genetic Algorithm Based Mapping and Routing Approach for Network on Chip Architecture", in *Chinese Journal of Electronics*, vol.19, No.1, Jan. 2010.
12. Glenn Leary, Krishnan Srinivasan, Krishna Mehta, and Karam S. Chatha, Member, IEEE. "Design of Network-on-Chip Architectures With a Genetic Algorithm-Based Technique", in *IEEE transactions on very large scale integration (vlsi) systems*, vol. 17, no. 5, may 2009.
13. Tang Lei, Shashi Kumar, "A Two-step Genetic Algorithm for Mapping Task Graphs to a Network on Chip Architecture".
14. Palesi, M., Daneshalab, M.: "Routing Algorithms in Network-On-Chip." *Springer Science + Business Media, New York* (2014).
15. Luca Benini, Giovanni De Micheli, "Network on Chips: A New SoC Paradigm", *IEEE Computer*, January 2002, pp. 70-78.
16. Nan Jiang et al., "A detailed and flexible cycle-accurate Network-on-Chip simulator," *2013 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, Austin, TX, 2013, pp. 86-96.
17. Andrew A. Chien and Jae H. Kim "Planar-Adaptive Routing: Low-cost Adaptive Networks for Multiprocessors"
18. Xu, Yongfeng, Jianyang Zhou, and Shunkui Liu. "Research and analysis of routing algorithms for NoC." *2011 3rd International Conference on Computer Research and Development*. Vol. 2. IEEE, 2011.
19. Myung, Wooshik, Zhao Qi, and Ma Cheng. "Performance Analysis of Routing Algorithms in Mesh Based Network on Chip using Booksim Simulator." *2019 IEEE International Conference of Intelligent Applied Systems on Engineering (ICIASE)*. IEEE, 2019.
20. Venkataraman, N. L., R. Kumar, and P. Mohamed Shakeel. "Ant lion optimized bufferless routing in the design of low power application specific network on chip." *Circuits, Systems, and Signal Processing* 39.2 (2020): 961-976.
21. Ortín-Obón, Marta, et al. "Analysis of network-on-chip topologies for cost-efficient chip multiprocessors." *Microprocessors and Microsystems* 42 (2016): 24-36.
22. Sharapov, R. R. "Genetic Algorithms: Basic ideas, Variants and Analysis, Vision Systems: Segmentation and Pattern Recognition." G. Obinata and A. Dutta (Ed.) (2007).
23. Biniha, S., and S. Siva Sathya. "A survey of bio inspired optimization algorithms." *International journal of soft computing and engineering* 2.2 (2012): 137-151.
24. Hemani, Ahmed, et al. "Network on chip: An architecture for billion transistor era." *Proceeding of the IEEE NorChip Conference*. Vol. 31. No. 20. sn, 2000.
25. Jain, Lavina, et al. "NIRGAM: a simulator for NoC interconnect routing and application modeling." *Design, automation and test in Europe conference*. IEEE, 2007.
26. Ohsaki, M. "Genetic algorithm for topology optimization of trusses." *Computers & Structures* 57.2 (1995): 219-225.
27. Braun, Heinrich. "On solving travelling salesman problems by genetic algorithms." *International Conference on Parallel Problem Solving from Nature*. Springer, Berlin, Heidelberg, 1990.
28. Inam, Omair, Sharifa Al Khanjari, and Wim Vanderbauwhede. "Shortest path routing algorithm for hierarchical interconnection network-on-chip." *Procedia Computer Science* 56 (2015): 409-414.
29. Latif, Jawwad, et al. "Design Trade off and Performance Analysis of Router Architectures in Network-on-Chip." *FNC/MobiSPC*. 2015.
30. Yaghini, Pooria M., Ashkan Eghbal, and Nader Bagherzadeh. "On the design of hybrid routing mechanism for mesh-based network-on-chip." *Integration* 50 (2015): 183-192.
31. Chen, Yu-Yin, et al. "Path-diversity-aware fault-tolerant routing algorithm for network-on-chip systems." *IEEE Transactions on Parallel and Distributed Systems* 28.3 (2016): 838-849.
32. Ascia, Giuseppe, et al. "Implementation and analysis of a new selection strategy for adaptive routing in networks-on-chip." *IEEE Transactions on Computers* 57.6 (2008): 809-820.
33. Agarwal, Niket, et al. "GARNET: A detailed on-chip network model inside a full-system simulator." *2009 IEEE international symposium on performance analysis of systems and software*. IEEE, 2009.
34. Masum, Abdul Kadar Muhammad, et al. "Solving the vehicle routing problem using genetic algorithm." *International Journal of Advanced Computer Science and Applications* 2.7 (2011): 126-131.
35. Abdullah, Nibras, et al. "Genetic-based routing algorithm with priority constraints." *International Journal of Networking and Virtual Organisations* 17.1 (2017): 3-16.
36. Man, Kim-Fung, Kit Sang Tang, and Sam Kwong. *Genetic algorithms: concepts and designs*. Springer Science & Business Media, 2001.
37. Paul, Tarak Nath, and Abhoy Chand Mondal. "Set of shorter paths using genetic algorithm and evaluating network delay." *2015 International Symposium on Advanced Computing and Communication (ISACC)*. IEEE, 2015.