# A Single-Phase Cascaded 19 Level Inverter Based on a New Basic Unit with Reduced **Number of Power Switches**



# Engineering

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Preeji. k. k

PG Student [PE], Electrical and Electronics Department, Calicut University

Radhika Somakumar

Assistant Professor, Electrical and Electronics Department, Calicut University

# **ABSTRACT**

Recently Multilevel inverters become a feasible solution to improve the power with a comparatively less stress on the components and with very easy control systems. The family of multi-level inverters has emerged as the solution for high power applications since implementation via a single power semiconductor switch directly in a medium-voltage network is hard work. In this paper, a new cascaded 19 level inverter is proposed. A new basic unit is proposed and the chosen basic unit topology can generate only positive voltage levels at the output thus in order to produce both positive and negative voltage levels at the output an H bridge is added to the basic unit. This proposed new topology of multi-level inverter requires less number of dc voltage sources, power switches and driver circuits as compared to conventional topologies. Thus mainly required installation space and total cost get reduced. The validation of  $proposed\,19\,level\,inverter\,is\,verified\,with\,simulation\,result\,using\,MATLAB\,software.$ 

#### I.INTRODUCTION

Now a day's multi-level inverters are finding increased attention in industry as the preferred choice of electronic power conversion for high power applications. It is very well suited for applications in a variety of industries involving the field of transportation and energy management. Multi-level inverters have been applied to different high power applications, such as railway traction application, large motor drives, high voltage DC transmission (HVDC), unified power flow controller (UPFC) and static synchronous compensator. Multilevel inverter generates better output waveforms with lower dv/dt than the standard inverter. The power quality of the multi-level inverter is high because of significant number of levels at the output step voltage thus the AC side filter can be reduced, this will reduce its cost and losses. Also multi-level inverter can operate with a lesser switching frequency comparing to other inverters, so the generated electromagnetic emissions by the multilevel inverters are very weak. Furthermore, multilevel inverter can be directly connected to high voltage sources without using the help of transformers.

Since 1975 the concept of multilevel converters has been introduced. The word multilevel start with the three-level inverter. Subsequently various multilevel inverter topologies have been developed. However, the basic idea of a multilevel inverter is to use a series connection of power semiconductor switches with various low voltage dc voltage sources to carry out the power conversion by generating a stepped staircase like voltage waveform.

Currently, large number of circuit topologies exist for multilevel inverters. Among them the three topologies are very popular. They are the neutral point clamped (NPC) topology, cascaded H-bridge (CHB) topology and the flying capacitor (FC) topology [1]-[3]. Out of these inverter topologies, cascaded multilevel reaches the higher output voltage, higher power levels and higher reliability because of its modular topology. Cascaded multilevel inverters are based on series connection of several power switches and dc voltage sources. One of the advantages of this type of multilevel inverters is that it need less number of components compared to the diode clamed or the flying capacitor multilevel inverters.

Cascaded multilevel inverter can operate as symmetric and asymmetric, magnitude of dc sources is the main difference between these two. In symmetric configuration the magnitude of dc voltage sources is same but in asymmetric configuration different magnitude of dc voltage sources are used. Thus asymmetric cascaded multilevel inverter can generate higher voltage levels because of the presence of different magnitude of dc voltage sources. Thus the installation space required and total cost needed for an asymmetric cascaded multilevel inverter is very less comparing to that of a symmetric cascaded multilevel inverter [5], [6]. A large

number of asymmetric configurations are also present in literature [1], [5] and [6]. But the dc voltage magnitude is very high in these papers

This paper proposes a new multi-level inverter topology using asymmetric configuration and all the switches used are unidirectional. A unidirectional switch is so called because it requires only one IGBT switch with an antiparallel diode and a driver circuit [7]- [9]. The proposed basic unit can generate 8 positive levels at the output and the levels can be further increased by adding dc voltage sources and corresponding switches in series with the basic unit. Since the chosen basic unit can only produce positive voltage levels at the output an H bridge should be added to the basic unit so that it can generate both positive and negative levels at the output. Finally using this basic unit and asymmetric configuration a 19 level inverter is developed.

### II. PROPOSED TOPOLOGY

To increase the output voltage levels by using reduced number of switches and dc voltage sources a new basic unit is proposed in this paper. Proposed basic unit is shown in fig.1. As shown in fig.1, the basic unit consist of four dc voltage sources and eight unidirectional power switches. It is an asymmetric multi-level inverter that is, magnitude of voltage sources is different. Here voltage source V<sub>1</sub>' is 20V and all other voltage sources have magnitude of 40V.

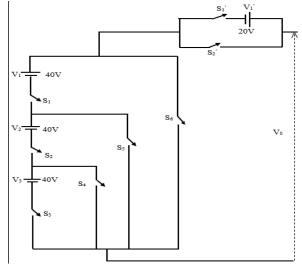


Fig.1 Basic unit

Table.1 shows the proposed basic unit power switches turn on and off states, where the basic unit is able to generate eight different voltage levels at the output. It is to be noted that the basic unit is only able to generate positive voltage levels at the output. In order to generate both positive and negative levels at the output an H bridge should be added in the output of the basic unit. By adding H bridge to this basic unit it can generate 15 levels at the output, circuit is shown in fig.2. When switches  $T_1$  and  $T_4$  are turned on we get positive voltage levels at the output, and if power switches  $T_2$  and  $T_3$  are turned on we get negative voltage levels at the output. Thus for generating 15 voltage levels at the output the proposed multilevel inverter topology only requires total 12 power semiconductor switches and 4 dc voltage sources which is very less compared to other conventional topologies.

Higher levels can be produced by adding additional dc voltage sources and switches in series to the basic unit. Fig.3 shows a 19 level inverter, formed by adding one additional dc voltage source  $V_4$  having magnitude of 40V and two more switches  $S_4$  and  $S_5$  in series to the basic unit. The circuit consist of 5 dc voltage sources and 14 unidirectional switches.

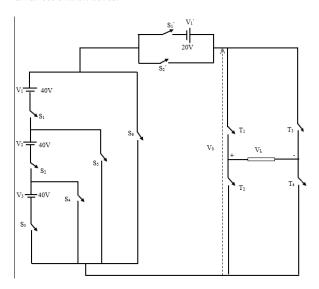


Fig.2 15-Level multilevel inverter

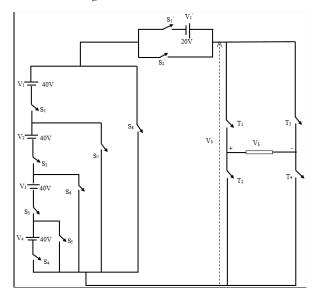


Fig.3 19 Level multilevel inverter

Table.1. Permitted turn on and off states for switches in the basic unit

State	Switch states								$V_0$
	S <sub>1</sub>	S <sub>2</sub> '	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	S <sub>5</sub>	S <sub>6</sub>	70
1	Off	On	Off	Off	Off	Off	Off	On	0
2	On	Off	Off	Off	Off	Off	Off	On	$V_1'$
3	Off	On	On	Off	Off	Off	On	Off	$V_1$
4	On	Off	On	Off	Off	Off	On	Off	$V_{1}' + V_{1}$
5	Off	On	On	On	Off	On	Off	Off	$V_1 + V_2$
6	On	Off	On	On	Off	On	Off	Off	$V_1' + V_1 + V_2$
7	Off	On	On	On	On	Off	Off	Off	$V_1 + V_2 + V_3$
8	On	Off	On	On	On	Off	Off	Off	$V_1'+V_1+V_2+V_3$

#### III. EXPERIMENTAL RESULT

In order to demonstrate the exact performance of the proposed multilevel inverter in producing the desired output voltage levels, help of experimental results have been used. Simulation of the 19 level multilevel inverters is done using MATLAB SIMULINK software and the diagram is shown in fig.4. Corresponding voltage with 19 levels and current waveform are obtained in the simulation successfully. RL load is used having values 70 ohms and 55mH respectively.

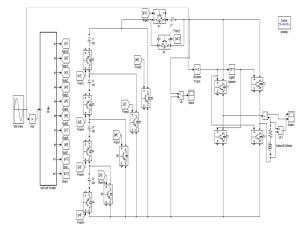


Fig.4 MATLAB Simulink model of 19-level multilevel inverter

In this, for switching normal fundamental frequency control technique is used. Asymmetric configuration is used with magnitude of  $V_1$  is 20V and all other dc voltage sources have magnitude of 40V and the generated output voltage have amplitude of 180V and current 2.57amperes.

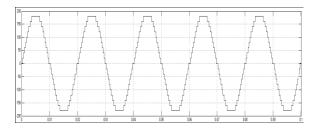


Fig. 5 Output voltage waveform of 19-level multilevel inverter

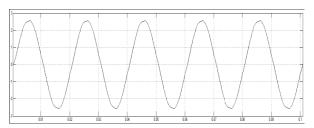


Fig. 6 Output current waveform of 19-level multilevel inverter

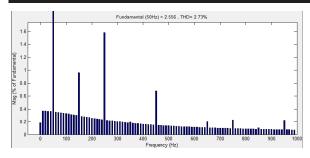


Fig. 7 Harmonic spectrum of output current waveform of 19level multilevel inverter

FFT analysis is used to evaluate the harmonic spectrum of voltage and current, and it can be seen that output current has distortion of 2.73%. The THD analysis is shown in fig.7. From the THD analysis it is clear that distortion is very less and distortion can be further reduced by increasing the levels of the multilevel inverter.

#### IV. CONCLUSION

A new basic unit with very low number of switches and dc voltage sources are introduced in this paper, which can generate higher levels at the output. Since this basic unit can only generate positive voltage levels at the output, an H-Bridge is added to this unit for producing both positive and negative levels at the output thus a sinusoidal like waveform is generated at the output. The levels can be increased further by simply adding more voltage sources and switches in series to the basic unit. Multi-level inverters have been applied to different high power applications like FACTS, HVDC, UPS, PV systems and Industrial drive applications. Comparing to other conventional inverter topologies, proposed new topology is better for all these applications in view of the fact that, its control complexity is very less, less size and cost. It also lowers the total harmonic distortion of output to a great extend thus minimize the size of filter.

### REFERENCES

- Boora, A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "Voltage sharing converter to supply single-phase asymmetric four level diode clamped inverter with high power factor loads," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2507–2520, Oct. 2010.
- 2. J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on natural point clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.
- E. Babaei, M. F. Kangarlu, M. Sabahi, and M. R. Alizadeh Pahlavani, "Cascaded multilevel inverter using sub-multilevel cells," *Electr. Power Syst. Res.*, vol. 96, pp. 101–110, Mar. 2013.
- F. Z. Peng, "multilevel inverters: a survey of topologies, control and applications" IEEE Trans. Ind. Applicat., vol. 49, pp. 724–738, august.2002
- S. Laali, K. Abbaszadeh, and H. Lesani, "Control of asymmetric cascaded multilevel inverters based on charge balance control methods," *Int. Rev. Elect. Eng.*, vol. 6, no. 2, pp. 522–528, Mar./Apr. 2011.
- E. Babaei and S. H. Hosseini, "Charge balance control methods for asymmetrical cascade multilevel converters," in Proc. ICEMS, Seoul, Korea, 2007, pp. 74–79.
- B. Ashok, A. Rajendran "Selective harmonic elimination of multilevel inverter using SHEPWM technique" IJSCE International journal soft computing, vol.3, issue.2, May 2013.
- E. Babaei, S. Alilu, and S. Laali, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3932–3939, Aug. 2014
- M.F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of sub-multilevel inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625–636, Feb. 2013.
- N. Farokhnia, S. H. Fathi, N. Yousefpoor, and M. K. Bakhshizadeh, "Minimizations of total harmonic distortion in a cascaded multilevel inverter by regulating of voltages DC sources," *IET Power Electron.*, vol. 5, no. 1, pp. 106–114, Jan. 2012.