Research Paper Engineering

Design of Efficient Binary Comparators Using Qca Module

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ABSTRACT

The project is based on Quantum-dot cellular automata (QCA) which is an emerging technology suitable for the development of ultra- dense low-power high-performance digital circuits suitable to carryout high performance. The Design of binary comparator is based on the QCA majority gate .With the help of theorems and corollaries the circuit is created .This paper proposes a new design approach oriented to the implementation of binary 64-bit full comparator using QCA majority gate module that exhibit significantly higher speed and reduced overall area. The design also reduces gate-count and improve processing speed. The 64 bit binary comparator can be used in various electronics application which reduce the power consumption and as well as switching speed.

KEYWORDS: majority gate, binary compatartor, QCA, theorems, corollaries, 64-bit

I. INTRODUCTION

Comparator is one of the fundamental building blocks in electronics devices. Comparator is mostly used in the ADCs that require high-speed, low-power consumption with small chip area. High-speed comparators in CMOS technologies suffer from low supply voltages especially when threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. So the designing of high-speed comparators is more challenging when the supply voltage is smaller. To compensate reduction of voltage usage large no of transistor is required which also means that more die area is required. Moreover low-voltage operation results in limited common-mode input range, which is important in high-speed ADC architectures, such as in flash ADCs. Binary comparator are made up from standard gate like

AND OR NOT that compare the digital signals present at their input terminals and produce an output depending upon the condition of those inputs. For example, if we want to add or subtract the value of input A and B the output of the given data comprises of three value [A=B, A>B A<B]. The digital comparator accomplishes this by using several logic gates that operate on the principles of Boolean algebra. The magnitude comparator is used to compare a set a variables for example A(a1 ,a2 ,a3.....an) against that of a unknown value B(b1, b2, b3....bn) to produce an output condition or flag.This project is based on the design of binary compactor with the use of majority gate module. The fundamental logic gates available within the QCA technology are the inverter and the majority gate (MG). The basic Boolean function in quantum cellular automata (QCA) is the majority gate. Theorems and corollaries are build with the majority gate to perform certain boolean operation.

II.MODULE DESCRIPTION

1. Majority QCA:

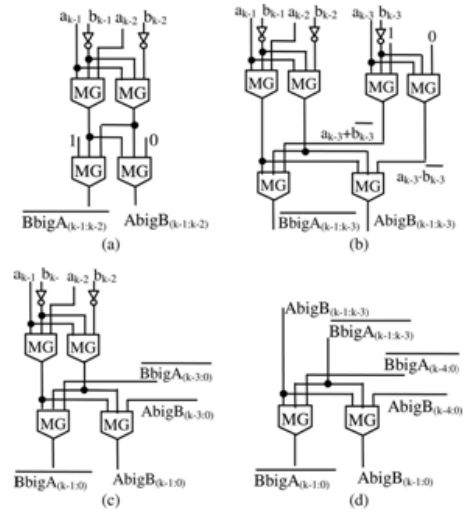
The majority gate(MG) have three inputs ports (a, b, c) .The MG performs the logic function reported in equation provided that all input cells are associated to the same clock signal clk x (with x ranging from 0-3), whereas the remaining cells of the MG are associated to

$$M(a,b,c) = a \cdot b + a \cdot c + b \cdot c$$

The latter can be rewritten as given in c i+2 = M (M (ai+1, bi+1, gi) M (ai+1, bi+1, pi) ci). In this way, the RCA action, needed to propagate the carry ci through the two subsequent bit positions, requires only one MG and conventional circuits operating in the RCA fashion require two cascaded MGs to perform the similar operation. The proposed n-bit adder is implemented by cascading n/2 ;2-bit modules as shown in Sum Chain. Having assumed that the carry-in of the adder is cin = 0, the signal p0 is not required and the 2-bit module used at the least significant bit position is modified. The sum bits are finally computed in Carry Chain.

2. Theorems And Corollaries:

Theorems and corollaries are the fundamental building blocks in the QCA technology. Majority gate (MG) is used to build up certain theorems and corollaries to perform certain logical operation .In our projects we have used four theorems[T1, T2, T3, T4] and two corollaries [C1, C2]. Inverter is used for executing different Boolean function.Wire is used to interconnect gates with each other. The theorems , corollaries and wire is used in the design of the binary comparator which has reduced the complexity and gate count. Furthermore clockcycle and reset is used to provide synchronization to the circuit.



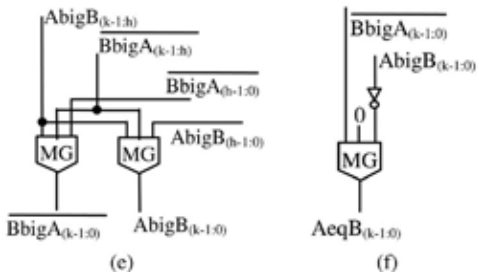


Fig: QCA modules: **(a) T1, (b) T2, (c) T3, (d) T4, (e) C1, (f) C2.**

iii.Cascade-Based (cb)full comparator

An n-bit CB full comparator designed as proposed here uses n/3 instances of T1 and/or T2; n/3 cascaded instances of T4 through which the signals AbigB(n–1:0) and BbigA(n–1:0) are computed; and one instance of C2, needed to compute also AeqB(n–1:0). Circles visible indicate the additional clock phases that have to be inserted on wires to guarantee the correct synchronization of the overall design. The CB full comparator was designed for operands word lengths ranging from 2 to 32 and using, for n > 2, the number of cascaded MGs within the worst computational path of a QCA design directly affects the delay caused. In fact, each MG introduces one clock phase in the overall delay. As always happens in CB computational design, the number of MGs within the computational path of the above described comparator linearly increases with n .The theorem here used were T1, T2, and T4 and corollaries C2. A 64 bit cascade design will process large amount of data within short time as it can take more input data than the 32bit cascade one.

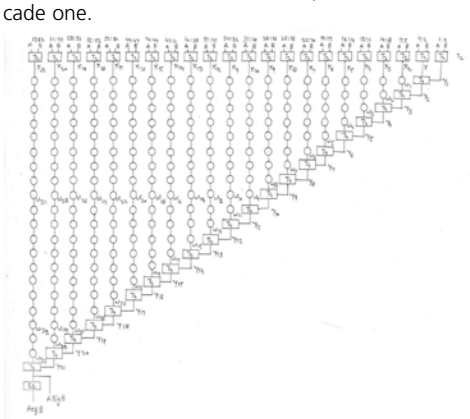


Fig: 64 bit Cascade-Based (CB) full comparator

iV.tree-Based (tb) architecture

A Tree-Based (TB) architecture and exhibits a delay that in theory logarithmically increases with n to achieve high speed. The intermediate results obtained are then further processed through a proper number of cascaded 2-input OR and AND gates are implemented by means of MGs having one input permanently set to 1 and 0, respectively. QCA implementations of binary comparators can be observed that they were designed directly mapping the basic Boolean functions consolidated for the CMOS logic designs to MGs and inverters. There are two types of tree-based architecture

i) Tree Based (A)-Architecture
ii)Tree-Based(B)-Architecture

The advantage of using TB-B architecture over TB-A architecture is that the gate count will be less compared to the latter one. TB-A architecture has more no of gate used and the clockphase takes more time to process the input. Whereas TB-B architecture is the better one since it has small number of gates and theorem used in it. The processing speed will be more in the case of B-architecture and the area used will be compact and efficient.

V.verilog

Verilog is one of the two major Hardware Description Languages (HDL) used .VHDL is the other one. Many feel that Verilog is easier to learn and use than VHDL Verilog HDL is a proprietary language of Cadence. It is a tool for design and verification of the analog circuit. The Front-end design associated with the VLSI uses Verilog code which has made the designing of IC more simple to the user .The theorems and corollaries have been implemented using Verilog program. The Verilog has made it easy to implement those logic to the circuit. The code and logic is implanted by verilog program.

Vi **software and hardware description**

1. Modelsim SE 6.4:

The software is used for verifying the program and circuit. The modelsim supports VHDL, system C system Verilog coding .It support RTL (Register Transfer Level), behavioural, gate level modeling of the Verilog program .Compilation of program and simulation of the program is executed in the modelsim . Modelsim is applicable for various other logical application. System level testing logical verification, vehavioural , post-place and route simulation are also executed using modelsim. The Verilog code is compiled and the waveform of the camparator can be analysed in the modelsim

2. Xilinx ISE Design 14.5:

Xilinx ISE is a software used to design FPGA product.It is used for designing and synthesizing HDL (Hardware Description Language) circuit. Time analysis of the circuit testing and examining of RTL diagram can also be performed with the features. Xilinx system generator is used for DSP and HDL coder. MATLAB coding can be integrated using xilinx .

3. Spartan3AN Stick Board /Spartan 6:

Spartan 3AN stick board is a USB enabled programming kit. Spartan 6 also supports the similar execution of the circuit. The configuration of the device is important while dumping of the code to the FPGA kit. The clock switch default value varies for different FPGA kit. Spartan 3AN

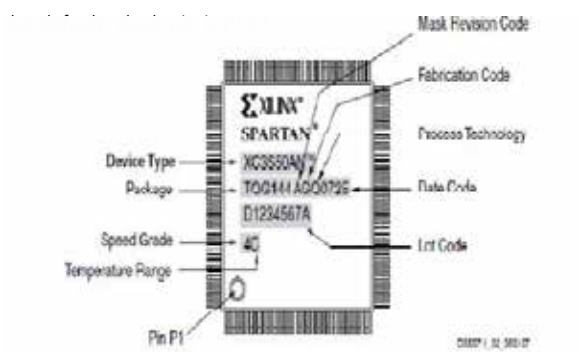


Fig: Spartan 3AN stick Board

Vii.result

The 64-bit binary comparator has been designed with the QCA based majority gate . The Cascade and Tree based design has been implemented by using the theorems and corollaries.



Fig: Spartan 3AN Stick Board configured

Vii. advantage Of 64-bit design over 32-bit

1. Low Computational Time
2. Very Compact
3. Switching Speed is improved

Viii.Application

1.DSP (Digital Signal Processing):

DSP is the mathematical manipulation of information signal .The Comparator is used in the field of signal processing. The processing will take less time and will perform better than 32 bit data comparator .The 64 Bit designed comparator can take more no. of inputs at a time and process large amount of data within a short period of time. The signal is represented in discrete form in both time and frequency domain .The purpose of DSP is to measure filter and compress real world analog signal .The signal from the sonar radar and tracking of robots are also applicable.In our real life we use different electronics which is a part of the system controlled and programmed by DSP.

2. Mobile Phone:

In our day today life we use mobile for communication by making a call which uses radio link whilst moving around the geographical area. It does so by connecting to a cellular network provided by a cell operator, that allow access to the public who are in different location through Switched Telephone Network (PSTN). In these mobile phones to reduce the area as well as the power an efficient comparator is required. So our adder design is used to mobile phones.

3. Satellite Application:

Satellites are used used in many purposes. Different types of satellite are used for certain application for instance military and Civilian satellite is used for defence and intelligence . Earth observation satellites are used in space and astronomical study. GPS and navigation satellite are dedicated for public use . weather satellites forecast and keep track of the climate . Satellite orbits vary depending on the application to maintain various task such as power generation ,telemetry and altitude For the monitoring of these activities , our adder will be used for some area efficient products.

ix.conclusion:

A new methodology useful to design binary comparators in QCA has been executed . The innovative formulations allow increased speed performances and reduced overall sizes achieved with respect to the existing competitors. Finally we designed and implemented the Cascaded based full comparator design and Tree Based comparator design.In future prospect 128 –bit and higher bit design of comparator can be be designed using this technology.

REFERENCES

[1] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernestein, "Quantum cellular automata." Year-2009 | | [2] M. T. Niemer , P. M. Kogge, "Problems in designing with QCAs: Layout = timing," Int. J. Circuit Theory, year-2001 | | | [3] W. Liu, L. Lu, M. O'Neill, and E. E. Swartzlander Jr., "Design rules for quantum-dot cellular automata, year-2011 | | | [4] K. Navi, M. H. Moaiyeri, R. F. Mirzaee, O. Hashemipour, and B. M. Nezhad, "Two new low-power full adders based on majority-not gates, year-2009 | | | [5] Title -Efficient design of a hybrid adder in quantum dot cellular automata, By V. Pudi and K. Sridharan, year-2012 |