Research Paper Engineering

Design and Simulation of High Speed,Low power Preamplifier Based CMOS Comparator Using 0.13µ technology

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ABSTRACT

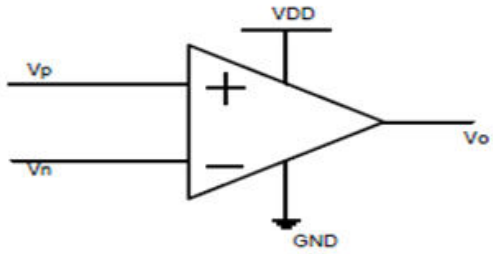
In today's world, where demand for portable battery operated devices is increasing, a major thrust is given towards low power methodologies for high speed applications. This reduction in power can be achieved by moving towards smaller feature size processes. This paper describes the design of high-speed CMOS voltage comparator with, propagation delay 1 ns and the sampling of 1 GHz. The comparator is designed in a 0.13 µm CMOS process with a Supply voltage of 1 V and -1 V consisting of a preamplifier and a latch stage followed by a buffer. The output buffer circuit consists of a full self biased differential amplifier and inverter. Here, preamplifier helps us to achieve high speed by increasing the difference between inputs signals, so faster decision can be taken at latch stage.

Keywords : Low voltage, High speed

I. INTRODUCTION

The comparator can be thought of as a decision making circuit. [1]The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison.

If the +, VP, the input of the comparator is at a greater potential than the -, VN, input, the output of the comparator is a logic 1, where as if the + input is at a potential less than the – input, the output of the comparator is at logic 0.



In its simplest form, the comparator can be considered as a 1-bit analog-digital converter. The presentation on comparators will first examine the requirements and characterization of comparators. It will be seen that comparators can be divided into open-loop and regenerative comparators. The open-loop comparators are basically op amps without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges that is a combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast. The input-referred latch offset voltage can be reduced by using the pre-amplifier preceding the regenerative output-latch stage. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also can reduce the kickback noise. However, the pre-amplifier based comparators suffer not only from large static power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain-to-source resistance rds due to the continuous technology scaling.

block diagram of High speed comparator is show below.

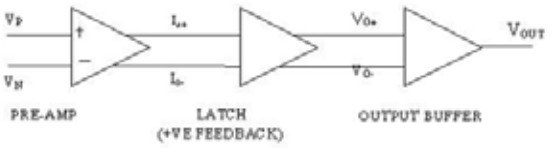


Fig.2 Block Diagram of High Speed Comparator.

In this paper a preamplifier based comparator is designed for gain more than 70db, propagation delay<1.5nsec for power supply of +/- 1v. This paper analyzes the systemic structure of the comparator, describes the circuit structure of the preamplifier, optimizes the gain and offset voltage, and designs the latch comparator.

The remaining sections of the paper are organized as follows. Section II describes the preamplifier based comparator, section III describes the design of comparator, Section IV describes the Pre layout Simulation of the CMOS Comparator in 0.13um technology. Section V describes results and conclusions.

II. COMPARATOR

The comparator consists of three stages as shown in fig:2; [2] the input preamplifier, a positive feedback or decision stage, and an output buffer. Differential amplifier will act as a preamplifier circuit.

Preamplifier:

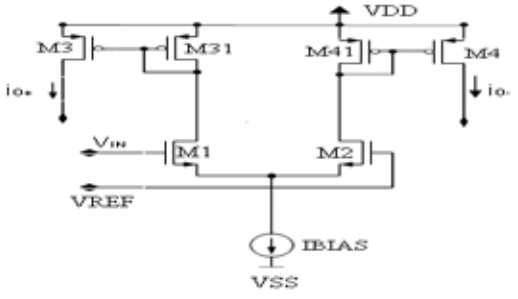


Fig.-3 Preamplifier

For the pre amplification stage, pre amplifier circuit is shown in fig 3. This circuit is a differential amplifier with active loads. The sizes of M1 and M2 are set by considering the diff-amp transconductance and the input capacitance. The transconductance sets the gain of the stage, while the input capacitance of the comparator is determined by the size of Ml and M2. Notice that there are no high-impedance nodes in this circuit, other than the input and output nodes.

LATCH – A decision circuit

This circuit must be capable of discriminating the mV signals. The circuit uses positive feedback from the cross-gate connection transistor to increase the gain of the decision element. Assume that $\beta_5 = \beta_8 = \beta_A$ and $\beta_6 = \beta_7 = \beta_B$. Assuming $io_+ >> i_{o-}$.

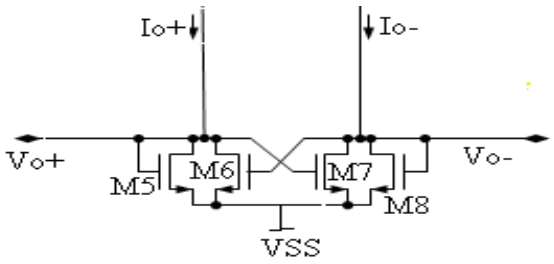


Fig.4 Latch

M8 are off, then vO- ~ 0V and vO+ is given by:

$$v_{O+} = \sqrt{\frac{2i_{O+}}{\beta_A}} + V_{THN}$$

If iO- increases iO+ decreases, switching takes place when VDS7 = VTHN6. At this point M6 start to take current away from M5. This decreases VDS5 and thus M7 turns off. Assuming that the maximum value of vO- or vO+ equal to 2VTHN, then M6 and M7 operate in either cutoff or triode regions. VDS7 reaches VTHN, and thus M7 enters the saturation region when current through M7 is:

$$i_{O-} = \frac{\beta_B}{2}(v_{O+} - v_{O-})^2 = \frac{\beta_B}{\beta_A} i_{O+}$$

Output Buffer

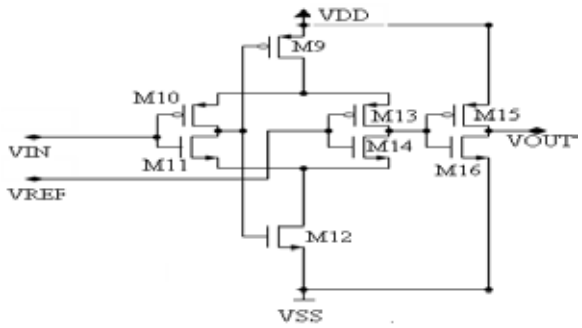


Fig. 5 Output Buffer of a Comparator

The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e. 0 or 5 V). The output buffer should accept a differential input signal and not have slew rate limitations. A self-biasing differential amplifier used as the comparator output buffer.

Current Mirror

The current source/sink is a basic building block in CMOS IC design and is used extensively in analog integrated circuit design. Ideally, the output impedance of a current source/sink should be infinite and capable of generating or drawing a constant current over a wide range of voltages. However, finite values of ro and a limited output swing required to keep devices in saturation will ultimately limit the performance of the mirror. The overall circuit is shown in fig-7.

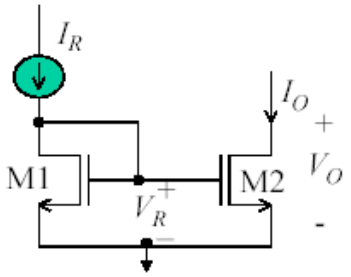
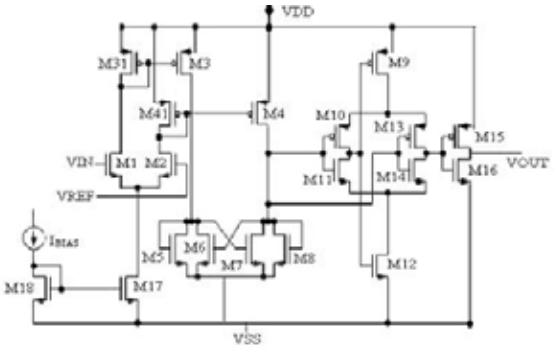


Fig-6 Current Mirror



III. Design of Comaparator

Figure 8 Ideal Comparator Transfer Characteristics

A comparator is a circuit that has binary output. Ideally its output shown in Figure 8 defined as follow.[1]

(1)

$$V_o = \begin{cases} V_{OH} & \text{if } V_{in+} - V_{in-} > 0 \\ V_{OL} & \text{if } V_{in+} - V_{in-} < 0 \end{cases}$$

Another non ideal characteristic of practical comparator is the presence of input offset. That the output does not change until the input difference reaches the input offset Vos. Figure 4 shows this transfer characteristic. Its output is defined as follows.[1]

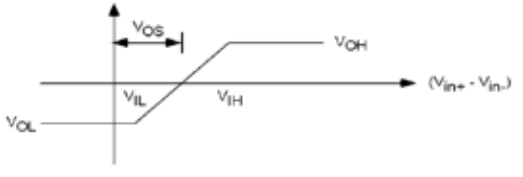


Figure 9 Transfer Characteristics of a comparator including

$$V_O = \begin{cases} V_{OH} & \text{if } (V_{in+} - V_{in-}) > V_{IH} \\ A_V(V_{in+} - V_{in-}) - A_V V_{OS} & \text{if } V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & \text{if } (V_{in+} - V_{in-}) < V_{IL} \end{cases}$$

Table I Design Specification

Parameter	Design Specification
Technology	0.13um
Propagation Delay	<1.5ns
ICMR	-0.5V to 0.5V
Gain	>70 dB
Power Supply	+/- 1V

IV. Prelayout Simulations

Prelayout simulation is carried out using the ELDO Spice in TSMC 0.13µm.The parameter used is BSIM3v3 Level – 53.

In this section static characteristics of comparator like offset, ICMR, Frequency Response and dynamic characteristics propagation delay is observed from the simulation.

Offset voltage is nothing but distance between the origin and the output.[3] Here the input voltage from -0.5V to0.5V for respective technology. From the simulation results shown in the figure 6 and 7 we observed the offset voltage is 39.28mv for 0.13 µm .

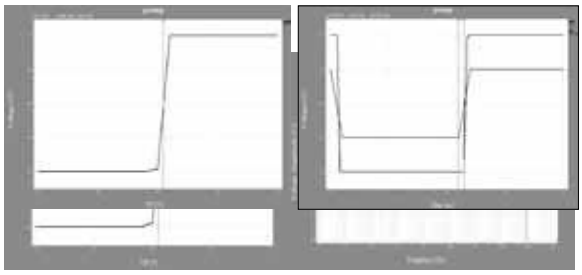


Figure 8 ICMR Figure 9 Frequency Response

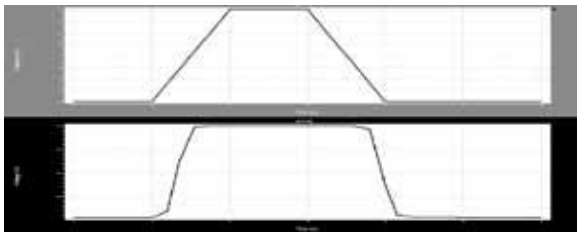


Figure 10 Sensitivity

III. Results and Conclusion

Table II Results

Parameter	Prelayout Simulation Results
Offset	49.18mV
Propagation Delay	473.56ps
ICMR	-0.2 V to 0.2 V
Gain	100dB
Speed	92.68Mhz

The comparator is designed in TSMC 0.13µm standard digital CMOS process. From the simulation circuit we observed the propagation delay of 0.48ns . The circuit operates at less than 100MHz with an offset voltage of 49.18mv. Higher speed can be achieved by using the clock comparator. Higher Gain of the comparator can also be achieved depending on the application be increasing the size of the transistor M3 and M4 and latch. Low Offset can be achieved by placing the proper offset compensation circuit in the comparator design.

REFERENCES

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