Research Paper Engineering

Analysis of Switched Capacitor Based 100 MS/s Pipeline ADC Using Time Shifted CDS Technique in 0.18 µm CMOS Technology

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ABSTRACT

A time-shifted correlated double sampling (CDS) technique is described to compensate for the finite opamp dc gain in a pipelined analog-to-digital converter (ADC). This technique can significantly reduce the errors due to the finite opamp gain without compromising the conversion speed. This is particularly useful for the design of low voltage and high-speed pipelined ADC where the trade-off of opamp dc gain and bandwidth is critical. This technique is useful in low gain opamp based switched-capacitor operation to achieve the equivalent accuracy that is traditionally possible only in high gain opamp based switched-capacitor operation. The entire Pipeline ADC was designed in TSMC 0.18µm 1.8V CMOS technology using Mentor Graphics Tool. Simulation results shows that it provides 100 MSample/S and conversion frequency of 9.86328125 MHz. Simulation of single block is analyzed in this paper.

Keywords : Time shifted CDS, Switch Capacitor, Sample and hold, MDAC architecture.

I. Introduction

Pipelined analog to digital converters (ADC) are very important building blocks in many electronic systems such as high quality video systems, high performance digital communication systems and high speed data acquisition systems. The rapid development of these applications is driving the design of pipeline ADC towards higher speed, higher dynamic range, lower power consumption and lower power supply voltage with the CMOS technology scaling. Scaling provides great challenges to conventional pipelined ADC designs which rely on high-gain operational amplifiers to produce high-performance converters, because at low power supply voltage and high speed operation, large open loop opamp gain is difficult to realize. So, the finite opamp gain is becoming a major obstacle in achieving both high speed and high resolution. Several analog and digital calibration techniques have been proposed to address the correction of the errors due to the capacitor mismatch and the finite opamp gain [2]-[4]. However, they faced practical limitations and added amount of complexity. Therefore, new, simple, and efficient opamp gain error correction techniques would be worthy of focused research.

In the following section, a time-shifted correlated double sampling (CDS) technique is described. The newly proposed technique is used for finite opamp dc gain compensation in the context of a low-voltage and high-speed pipelined ADC.

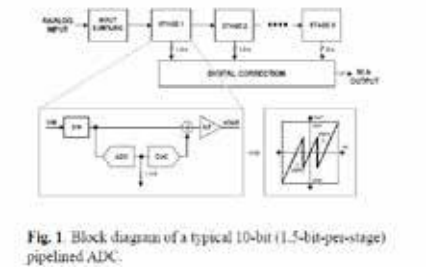

Fig. 1. Block diagram of a typical 10-bit (1.5-bit-per-stage) pipelined ADC.

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II. TIME-SHIFTED CDS TECHNIQUE

Block diagram of a conventional 10-bit pipelined ADC utilizing 1.5-bit-per-stage architecture is shown in Fig 1. This architecture is commonly used due to its nice trade-off between speed and power consumption at architectural level. It consists nine cascaded stages. In first 8 stages the input signal is first quantized by a sub-ADC (flash ADC), then the output digital code is converted back to an analog signal by a sub-DAC. This quantized analog signal is then subtracted from the input signal; a residue from the stage is amplified and then passed onto the next stage. 9th stage has only a 2-bit flash ADC. In switched-capacitor implementation, the functions of sub D/A conversion, subtraction, and amplification are combined together. Typical switched-capacitor implementation of this block called multiplying digital-to-analog converter (MDAC) is shown in Fig. 2. The output of this MDAC is given by

$$V_0 = \left(\frac{Cs + Cf}{Cf}\right) \cdot V_i - \left(\frac{Cs}{Cf}\right) \cdot V_R + e \qquad (1)$$

Where V_R is $\pm V_{ref}$,0 depending on the result of sub A/D conversion, and is e the error due to the finite opamp gain. It is given by

$$e = \frac{-1}{A}\left(1 + \left(\frac{Cs}{Cf}\right)\right) \cdot V_0 \qquad (2)$$

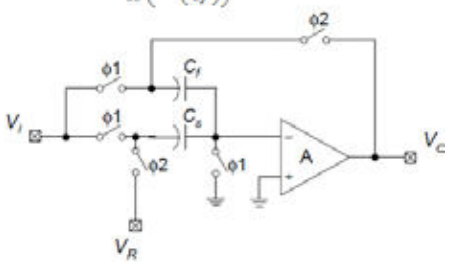

Fig. 2. A Typical MDAC in A Pipelined ADC with 1.5-Bit per-stage.

This error is inversely proportional to opamp gain e, and it will directly deteriorate the linearity of overall ADC. Fig.3 shows the proposed time-shifted CDS technique to be used in a 10-bit pipelined ADC. The proposed architecture has two pipeline paths working in parallel. One represents the predictive path which operates for the first five stages, and the other represents the main path which operates for all nine stages necessary for 10-bit ADC (1.5-bitper-stage). First five stages of the main pipeline are similar to their corresponding stages in the predictive pipeline and they share one set of stage sub-ADCs. Both pipeline paths process the same input signal from the first sample-and-hold (S/H) stage. But the signal in the main pipeline is delayed by half clock cycle (one phase) by an additional S/H following the first S/H. The gain error correction is done as follows: The input signal is first processed by the predictive pipeline, and the errors due to finite opamp dc gain are stored and then passed onto the corresponding stages in the main pipeline half clock cycle (one phase) later to cancel the gain errors of those stages. This approach effectively behaves as predictive CDS.

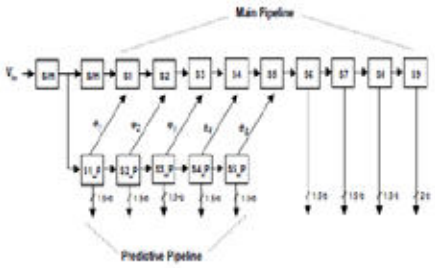

Fig. 3. Proposed Pipelined ADC Architecture.

In switched capacitor implementation of this architecture, the MDACs of predictive pipeline and main pipeline can be combined together. Fig.4 shows one such MDAC.

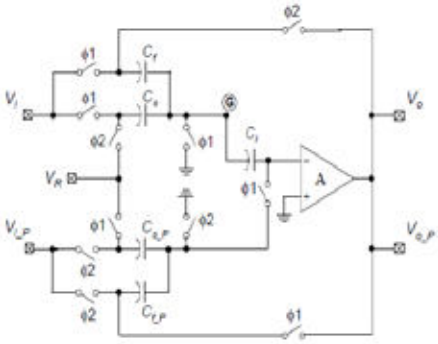

Fig. 4. Proposed MDAC Structure.

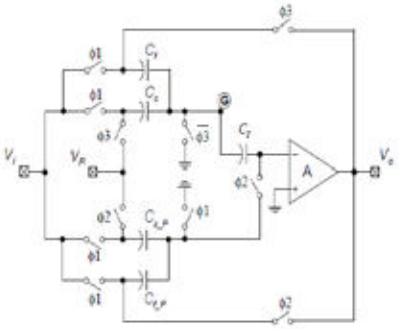

Fig. 5. MDAC Employing Conventional Predictive CDS Scheme.

V_i and V_0 are the input and output of one stage in main pipeline, whereas V_{i_P} and V_{0_P} are the input and output of the corresponding stage in predictive pipeline. The capacitors are chosen such that $C_{S\_P} = C_S = C_f = C_{f\_P}$. This MDAC employs a similar finite opamp dc gain error correction principle as the conventional predictive CDS technique [3]. In this technique, the sampling and amplifying operation is actually performed twice. The first operation is done by C_{f_p} and C_{S_P}.The resulted non-zero error voltage due to finite opamp dc gain at the negative input of opamp will be stored in C_I.Then during the second operation done by ϕ_2, C_f and C_I will be connected between the negative input of opamp and node G (the common node of C_f, ϕ_2). Through these operations, a much more accurate virtual ground than the negative input of opamp is created at node G for C_f and ϕ_2 if V_{0_P} and V_0 are close to each other. Thus the effect of finite opamp gain will be significantly reduced for the second operation.

The main difference between this proposed time-shifted CDS technique and conventional predictive CDS technique described in [5] is that the input has to be held constant over two operations in each stage for the conventional CDS technique [5], while in the proposed scheme the input signal goes through two separate paths, and the inputs of the MDACs in these two paths are allowed to be slightly different down the pipeline while allowing slightly less effective operation of CDS. If we were to apply conventional CDS technique directly to a pipelined ADC, we would need one extra clock phase to hold the input signal constant over two clock phases. The resulted three clock phase scheme puts a large penalty on the speed of A/D conversion which is unacceptable for the designs pursuing maximum speed. Fig (5) shows a possible MDAC scheme employing conventional CDS technique. There are three clock phases are used and the output capacitive load is doubled because two sets of capacitors sample at the same time. While for the proposed approach, only two clock phases are needed (unchanged from the regular switched capacitor circuit) and the effective capacitive output load is not increased as it would be in a standard three-phase operated predictive CDS. Therefore the proposed technique can compensate for finite opamp dc gain while maintaining the same speed potential and power dissipation as the regular MDAC without CDS. Only overhead is the need for two sets of capacitors in each MDAC, which would be necessary in all CDS schemes. Some design issues must be considered when applying the proposed architecture. First, since the inputs of MDAC are not the same for predictive path and main path, the effect of error correction won't be as good as conventional CDS technique as in [4] because the effect of error correction relies on the similarity of the inputs of two path. The output error in stage □in main pipeline is given approximately by

$$e_i = \frac{-i}{A^2}\left(1+\left(\frac{Cs}{Cf}\right)\right)\left[\left(1+\left(\frac{Cs+CI}{Cf}\right)\right)V_{oi}(n)-\left(\frac{CI}{Cf}\right)V_{oi}(n-1)\right] \quad (3)$$

Where is the output current in the main pipeline, and $V_{i}(n-1)$ 'is the main pipeline output of previous clock cycle. Here the error is inversely proportional to A^2. However it will increase linearly from stage to stage down the pipeline. This is because the difference between the outputs of the predictive path and main path will get larger from stage to stage down the pipeline. The second design issue is that the time-shifted CDS technique will add extra offset to sub-ADCs in main pipeline. The reason is that the MDACs in main pipeline need to use the digital code generated by the sub-ADCs in predictive pipeline, and this is equivalent to putting an offset to the sub-ADCs in main pipeline. This offset must be corrected; otherwise it will cause code error. Fortunately, pipelined ADCs normally have stage resolution redundancy and employ digital correction to correct the errors come from the stage sub-ADCs. Therefore they can tolerate large offset of sub-ADCs (for 1.5-bit-per-stage structure). For this reason, the proposed time-shifted CDS technique should not be used for too many stages, lest the accumulated error can overflow the bounds of digital correction and the linearity of overall ADC will be degraded. Another point to be careful about is the size of C_I. If C_I is too large, the gain error of predictive pipeline would be also large, then the effect of error correction is degraded.

If C_I is too small, the clock feed-through will change the charge stored in C_I .then the effect of error correction is also degraded. In a practical design, the size of C_I can be optimized via simulation.

III. Simulation Results

Fig. 6 shows input signal of 9.86328125MHz applied to Pipeline ADC.

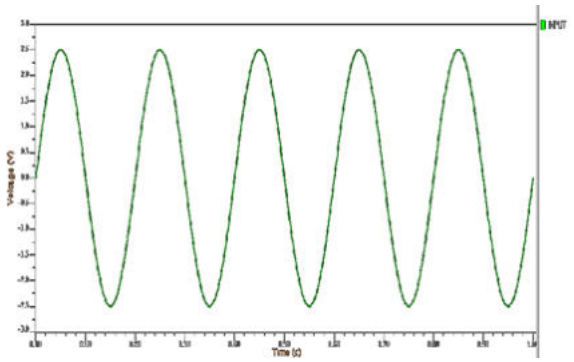

Fig.6. Input signal for Pipeline ADC

The Sample and Hold circuit is simulated with an input sinusoidal signal of frequency 9.86328125 MHz, 1.2VPP (peak to peak input voltage) and the common-mode voltage of 0.9V for different inputs using load capacitors 2.2 pF.

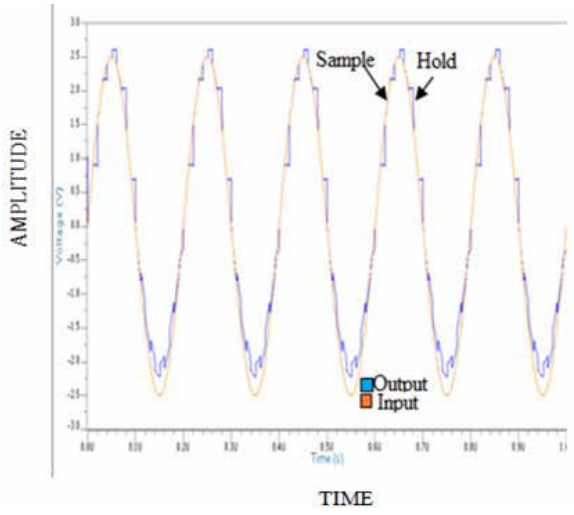

Fig. 7. Transient simulation of the Sample and Hold (fm=9.86328125MHz, fs = 100MHz, common-mode input voltage = 0.9V)

Fig.8 determines the intermediate MDAC output signal which is then multiplied by 2 and passed to the next stage .Digital Output of the single stage is shown in Fig.9 which shows Vdd as logic 1 and Vss as logic 0. Finally Simulation Summary is shown in Table 1.

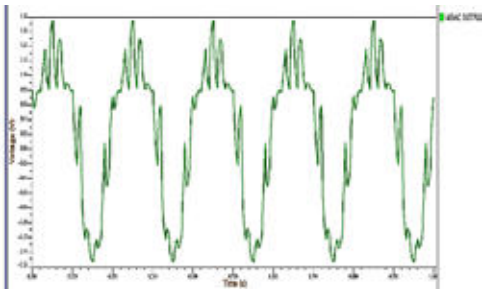

Fig.8. Transient simulation of the intermediate MDAC

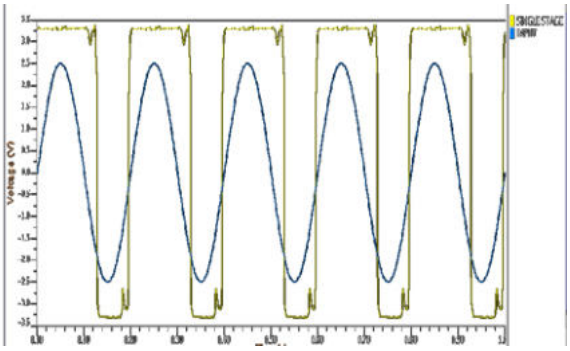

Fig.9. Digital Bits output of the Single stage Pipeline ADC

Table 1. Summuray Of ADC Simulation Results

1	Technology	0.18 µm
2	Supply voltage	1.8V
3	Samples	100 M Samples/Second
4	frequency	9.86 MHz
5	Settling time	3.2ns
6	Power dissipation	7.6mW

IV. Conclusion

New time-shifted CDS technique that compensates for the finite opamp gain in the design of a pipelined ADC is described. The finite opamp gain error can be reduced significantly without increasing the power dissipation or adding extra clock phase. This new CDS technique demonstrates that CDS can be applied in the first few stages of pipelined ADC without the increased capacitive load or the need for extra clock phase as far as the accumulated error stays within the limits of digital redundancy budget. This structure can be further modified to get higher samples. In future further modified structure can be implemented to achieve higher gain also, which enhances the circuit performance.

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