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Effect of Aspect Ratio W/L ,Body Bias ,and supply Voltage (vDD) for NMOS & PMOS transistor.

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ABSTRACT

We present a new approach for the estimation and optimization the effect of biasing voltage (VDD), Body bias , Aspect ratio (W/L) on NMOS and PMOS transistor. The main purpose of this paper is to demonstrate a systematic approach to design high performance high speed switching applications in digital circuit. MOSFET performance on body bias is experimentally evaluated with various channel-doping profiles to provide guidance for channel engineering in a forward body-biasing scheme. Forward body bias improves VTH in NMOS and PMOS transistor. A reverse body bias has the opposite effect and also enhances the band-to-band tunneling current, resulting in leakage current (I¬OFF¬¬) increase. Therefore, a forward body-biasing scheme is preferable in some important aspects. In previous studies, VF and VR were separately applied to the same device and the resultant performance characteristics were compared. This method is incorrect, however, because of the vastly different values of VTH. Various characterization has been performed on 0.18 nm NMOS & PMOS devices for different substrate voltage values VBS and for various Aspect ratio W/L at different biasing voltage in order to determine the difference between experimental results and theory. Both experimental results and simulations outline change in ID drain current with the change in substrate voltage (VBS) at constant aspect ratio and VDD. charge controlled devices which means that their output current is proportional to the charge established in the semiconductor by the control electrode. MOSFET technology for digital and power applications is driven by two of their major advantages over the bipolar junction transistors. One of these benefits is the ease of use of the MOSFET devices in high frequency switching applications. The MOSFET transistors are simpler to drive because their control electrode is isolated from the current conducting silicon, therefore a continuous ON current is not required. Once the MOSFET transistors are turned-on, their drive current is practically zero. MOSFETs have a resistive nature. The voltage drop However, because of limitations of the fabrication process, The effect of the geometry aspect ratio, W/L, on characteristics of the 0.18 nm gate are evaluated with reference to various device characteristics and the circuit properties, However, for a digital circuit configuration, the transient response of the circuit relies on the charge/discharge capability of the transistor. Thus, a device with a large aspect ratio will be more suitable for digital applications. The most popular circuit solutions and their performance are analyzed, including the effect of body Bias, Aspect ratio and Biasing Voltage

Keywords : ID Drain current, NMOS & PMOS, Aspect Ratio, Biasing Voltage and Forward & Reverse body bias.

1. INTRODUCTION

MOSFET is an acronym for Metal Oxide Semiconductor Field Effect Transistor and it is the key component in high frequency, high efficiency switching applications across the electronics industry [4] The bipolar and the MOSFET transistors exploit the same operating principle. Fundamentally, both type of transistor across the drain source terminals of a MOSFET is a linear function of the current flowing in the semiconductor [4]

As CMOS technology moves toward the deep submicron feature sizes, Meanwhile, ICs are becoming denser and larger which further increases their quiescent currents. On the other hand, for deep submicron technology circuits, the voltage has been reduced while the resistance remains relatively constant. For ID testing to continue to be effective in future technologies, techniques to control the defect free quiescent current must be developed. As well as for reducing standby power [2]

Some potential solutions have been suggested. These solutions include among others:

(1) Cooling down device during testing.
(2) Partitioning network and performing ID test on individual segment of design.
(3) Using state dependent ID instead of a single current threshold
(4) Architectural changes such as using dual threshold devices.
(5) Reverse biasing the substrate during testing and use of alternative technologies;

In this paper, we examine the effect of body biasing on the effectiveness of ID testing in technology. We have used extensive SPICE simulation to characterize the off current in 0.18 nm technology MOS devices Results on reduction drain current ID and input state dependence are reported and discussed.

2. DRAIN CURRENT

The Drain current in devices NMOS & PMOS consist of various components that are due to several physical phenomena. Of these components, the most relevant are Illustrated Depending on the value of the gate-source voltage (VGS) .some components are more dominant than others. In the off state, VGS = 0 or is slightly negative (positive) for NMOS

(PMOS) transistors. In this region, the most important components are source current (Is) and Drain current (ID). The latter component is function of the geometry of the device, as well as the voltage across this device, VBS. Device simulations were run on predictive 0.18nm NMOS transistors (aspect ratio w/l =1.5,VDD=1.8v)and PMOS transistor (aspect ratio w/l=3,VDD = 1.8v) at room temperature for both positive & negative variation of VBS from (-1.8 to +1.8) Drain current has been measure and graph plotted figure 1 shown for NMOS for +ve & -ve value of VBS Simulation result is shown in Table 1. The graph plotted in figure 2 shown for PMOS for +ve & -ve value of VBS .Simulation result is shown in Table 2

Table 1 & Graph 1 for NMOS positive & negative Value

S.NO	VBS	VGS	ID (Drain current)
1	0.2v	0v	4.05E-05
2	0.4v	0v	1.14E-05
3	0.6v	0v	5.49E-07
4	0.8v	0v	7.72E-09
5	1v	0v	7.68E-11
6	1.2v	0v	7.24E-13
7	1.4v	0v	6.79E-15
8	1.6v	0v	6.36E-17
9	1.8v	0v	**5.96E-19**

NMOS for positive value of V_{BS} NMOS for negative value of V_{BS}

S.NO	VBS	VGS	ID (Drain Current)
1	-0.2v	0v	1.10E-04
2	-0.4v	0v	1.48E-04
3	-0.6v	0v	1.86E-04
4	-0.8v	0v	2.25E-04
5	- 1v	0v	2.65E-04
6	- 1.2v	0v	3.05E-04
7	- 1.4v	0v	3.45E-04
8	- 1.6v	0v	3.85E-04
9	- 1.8v	0v	4.25E-04

In fig. 1 the characteristics curve has shown the different behavior for positive and negative values. Logarithmic behave for positive value and linearly decrease for negative value. These behave shows the majority charge carrier electrons inside the NMOS and followed by the Fermi Dirac statistics. During this phenomenon the vacancies created from the valence band to conduction band and the extra energy to cross the Fermi gap. ID values are starting to decrease from 0.5V and finally found the minimum value at 1.8VBS while linearly decreases for negative value in NMOS.

Table 2 & Graph 2 for PMOS Positive & Negative value

S.NO	VBS	VGS	ID (Drain current)
1	0.2v	1.8v	-1.17E-16
2	0.4v	1.8v	-1.22E-14
3	0.6v	1.8v	-1.27E-12
4	0.8v	1.8v	-1.30E-10
5	1v	1.8v	-1.19E-08
6	1.2v	1.8v	-6.56E-07
7	1.4v	1.8v	-8.03E-06
8	1.6v	1.8v	-2.46E-05
9	1.8v	1.8v	-4.72E-05

PMOS for positive value of V_{BS} PMOS for negative value of V_{BS}

S.NO	VBS	VGS	ID (Drain current)
1	-0.2v	1.8v	-1.07E-20
2	-0.4v	1.8v	-1.03E-22
3	-0.6v	1.8v	-9.85E-25
4	-0.8v	1.8v	-9.45E-27
5	- 1v	1.8v	-9.06E-29
6	- 1.2v	1.8v	-8.69E-31
7	- 1.4v	1.8v	-8.33E-33
8	- 1.6v	1.8v	-7.97E-35
9	- 1.8v	1.8v	-8.48E-37

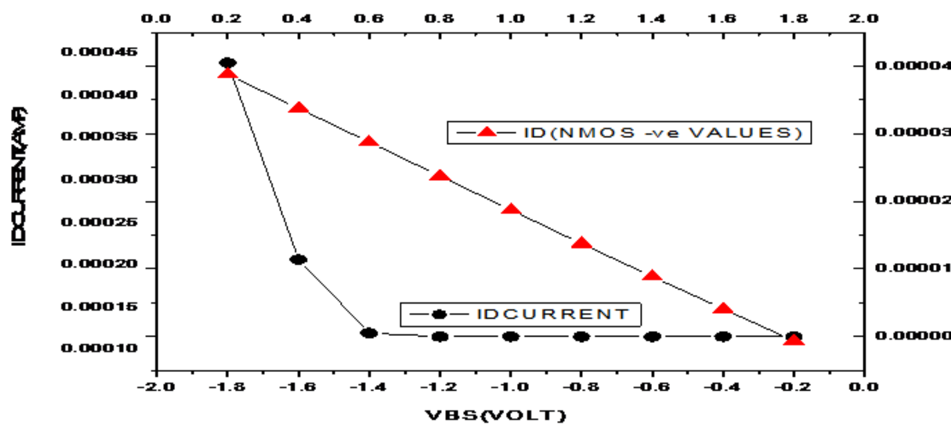

Fig. 1 Characteristics curve for NMOS,(W/L=1.5,VDD=1.8V)

In fig 2 the characteristics curve has shown the reverse be-

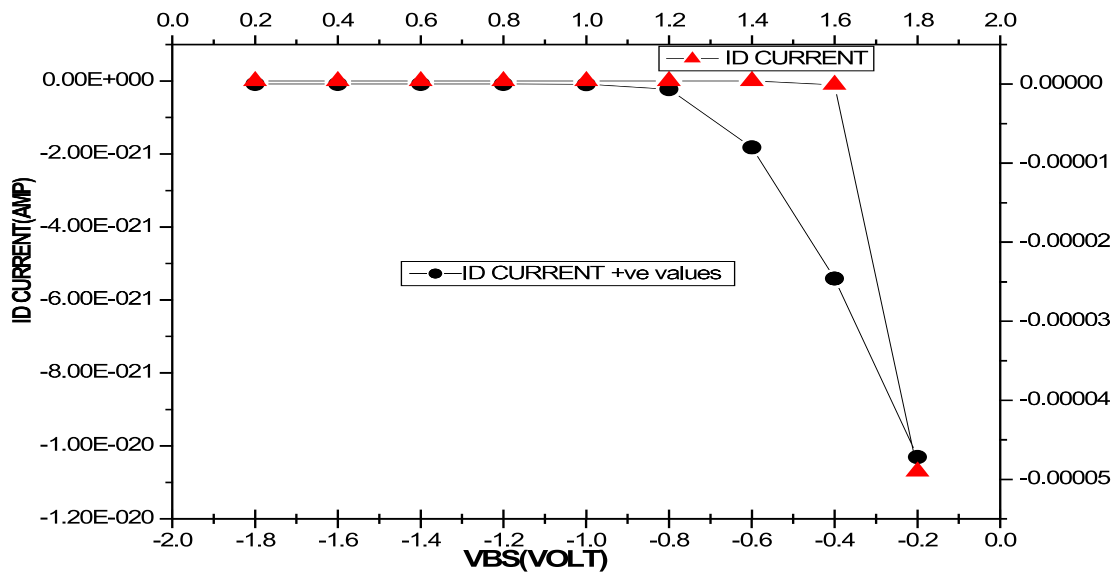

Fig.2 Characteristics curve for PMOS,(W/L=3,VDD=1.8V)

havior for positive and negative values. These behave shows the minority charge carrier electrons inside the NMOS. Doping concentration effect the ID Drain Current in these characteristics curve. These behave shows the majority charge carrier electrons inside the NMOS

3. EFFECT OF BODY BIAS ON LEAKAGE COMPONENTS

Understanding the relative importance of key leakage components in scaled technologies and how each of these components is affected by body bias is a necessary prerequisite for developing a body bias based techniques to limit leakage.

3.1. Sub-threshold Leakage

Sub-threshold current is the weak inversion conduction current that flows between the source and drain of a MOSFET when the gate voltage is below V_{TH}. Due to low threshold voltages, sub threshold leakage dominates the off-state leakage of current MOSFETs. [1]. This effect is referred to as Drain-Induced Barrier Lowering (DIBL) and is responsible for a reduction in threshold voltage at high drain biases, Sub threshold leakage is also modified by the body effect. Reverse biasing the substrate to source junction of a MOSFET widens the bulk depletion region. This increases the threshold voltage and thereby reduces the sub-threshold leakage..The subthreshold leakage of a MOS device taking into account weak inversion, DIBL, and the body effect [6]

3.2. Source/Drain Junction Band-to-Band Tunneling Leakage

MOS transistors have reverse biased *pn* junctions from the drain/source to the well. The reverse biased *pn* junctions give rise to minority carrier diffusion/drift current near the edge of the depletion region. This *pn* junction reverse bias leakage is a function of junction area and doping concentration. But if both the *n*- and *p*- regions are heavily doped dominates the *pn* junction leakage [3] , the high electric field across the reverse-biased *pn* junction causes electrons to tunnel from the valence band of the *p*-region to the conduction band of the *n*-region[6] .The exact dependence on Voltage applied depends on the doping profile in the substrate. As stronger halo implants are used and as the halo implants are located closer to the source/drain region, much forward bias will cause excessive *pn* junction leakage as the junction becomes more weakly reverse biased. [2]

3.3. Gate Leakage

The reduction of gate oxide thickness coupled with the resultant high electric field across the oxide results in significant tunneling through the gate oxide in scaled devices. There are three components of gate leakage: I_{GD} is the gate leakage between the gate and the drain, I_{GS} is the gate leakage between the gate and the substrate; and I_{GS} is the gate leakage between the gate and the source. [5]

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We have observed that the charge carrier mobile and immobile ions are playing a vital role for the conduction of current in both series of MOS. Leakage effect has been observed; increases VBS potential increases the leakage current in CMOS. For the best higher circuit designing technology with higher switching speed VBS should be maximum and minimum for NMOS and PMOS respectively.

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