Research Paper

Engineering

Four-quadrant Analog Multiplier Based on a Flipped Voltage Follower Cell in 0.18µm CMOS Technology

*Nipa B. Modi  **P. P. Gandhi

* PG Student L. C. Institute of Technology, Bhandu
** Assistant Professor, L. C. Institute of Technology, Bhandu

ABSTRACT

In this paper CMOS voltage mode four quadrant analog multiplier circuit is proposed. It is based on FVF cell. The multiplier combines the features of both, the Flipped voltage follower cell and Square rooting circuit. The circuit is designed and analyzed in 0.18µm CMOS process model and simulation results have shown that, under single 0.9V supply voltage, and it consumes only 29µw quiescent power.

Keywords : analog multiplier, four-quadrant, flipped voltage follower, square rooting circuit

I. INTRODUCTION

Multiplier is an essential part for many analog applications. The multiplier performs a linear product of continuous signals x and y yielding an output z = Kxy, where K is a constant with suitable dimension. Varieties of multipliers have been designed for different optimization objectives [1][6]. It is used in many applications such as voltage-controlled amplifier, ring modulator, product detector, frequency mixer, squelch, analog computer, analog signal processing, automatic gain control, true RMS converter, analog filters. These applications are required to operate in low voltage environment for improving their power efficiency and incorporating with mixed signal systems to be used in portable application. There are classified in several types of analog multipliers namely, single quadrant analog multiplier, two quadrant analog multiplier and four quadrant analog multiplier. A four quadrant multiplier is one where inputs and outputs may swing positive and negative, while two-quadrant multiplier only has one input that has one polarity. Besides that, single quadrant analog multiplier only has inputs and outputs with only one polarity. To implement the multipliers in IC technologies, the Gilbert cell is a popular and oldest structure in IC technologies due to wide dynamic range and high frequencies performance. In CMOS technology, approaches which are important for most applications are CMOS multipliers using MOS transistors working in saturation region, and non-saturation region [8].

In this paper, we proposed a CMOS analog multiplier classified as Type IV, which has single low supply voltage, and is compatible with low-power operation. In order to get a lower power supply and power consumption, concentrating on circuit topologies, which circuit cell called "flipped voltage followers"(FVF). It has been used for design since it needs only a supply voltage of VTH – Veff, where VTH is the threshold voltage and Veff(=VGS – VTH) is the effective gate voltage.

The paper is divided into four sections. Second section discusses the basics of multiplier operation and overview of Flipped voltage follower and Square rooting circuit. Third section includes how to design the Multiplier based on FVF cell circuit. In fourth section, simulation results are presented. In fifth section, conclusion regarding the multiplier is discussed.

II. PRINCIPLE OF OPERATION

In order to make a new circuit design, MOS Transistor is an important piece of device used in this study. By using drain circuit equation of MOS Transistor which works on saturated range. There are two styles of a squaring circuit and both of them work on the basic of the same principle. The relationship of the drain current is given by:

\[ I_D = K_N(V_{GS} - V_{TN})^2; V_{GS} > V_{TN}, V_{DS} \geq V_{GS} - V_{TN} \] (1)
\[ I_D = K_P(V_{GS} - V_{TP})^2; V_{GS} > V_{TP}, V_{DS} \geq V_{GS} - V_{TP} \] (2)

Where, K_N and K_P are the transconductance parameter of NMOS and PMOS, respectively VTN and VTP are the threshold voltages of NMOS and PMOS, respectively. VGS and VDS are the gate-to-source voltage and the drain-to-source voltage, respectively.

III. Flipped voltage follower cell

The circuit in Fig. 1 is source follower where the current through transistor M1 is held constant, and not depend on the output current. It could be described as a voltage follower with shunt feedback. Neglecting body effect and the short-channel effect, VGSM1 is held constant, and voltage gain is unity. Circuit is able to source a large amount of current, but its sinking capability is limited by the biasing current source Ib, due to the low impedance at the output node.

\[ R_{O2} = \frac{1}{R_{O1} + R_{O2} + R_{O3}} \] (3)

Where , gme and gm2 are the transconductance of the transistors M1 and M2 respectively, and roi is the output resistance
The equation (3) shows that the circuit has very low output resistance usually required for voltage source. This value is in the order of 20-100 Ohms. The relationship of the voltage at the terminal $V_o$ to bias current of $M_3$.

2) Square rooting circuit

The square-rooting circuit shown in Fig.2 consists of an MOS transistor ($M_3$) and the flipped voltage follower ($M_1$ and $M_2$). The transistor $M_3$ in fig.3 is used as a simple current-to-voltage converter. When source terminal voltage of $M_3$ is equal to $-V_{TN}$ therefore, the current of equation shown as:

$$I_n = I_{D3}$$ \hspace{0.5cm} (4)

When $I_{os} = K_n(V_0 - (-V_{TN}) - V_{TN})^2 = K_nVO^2$. The relationship between input current ($I_n$) and output voltage ($V_o$) can be expressed as:

$$V_o = \sqrt{\frac{I_n}{K_n}}$$ \hspace{0.5cm} (5)

V. Circuit design

Fig.3 shows the circuit of four quadrant analog multiplier based on FVF cell consisting of combination of common source amplifier with a differential voltage controlled square rooting circuit.

The multiplier circuit formed by common source amplifiers $M_1$-$M_4$ connected pair of differential flipped voltage followers (DFVF). $M_5$-$M_7$ and $M_8$-$M_{10}$. All transistor work on saturation region, the drain currents of $M_1$ to $M_4$ are given as:

$$I_{D1} = K_n(V_1 - V_{TN})^2$$ \hspace{0.5cm} (6.a)

$$I_{D2} = K_n(V_1 - V_{TN})^2$$ \hspace{0.5cm} (6.b)

$$I_{D3} = K_n(V_2 - V_{TN})^2$$ \hspace{0.5cm} (6.c)

$$I_{D4} = K_n(V_2 - V_{TN})^2$$ \hspace{0.5cm} (6.d)

From (a) and (b), we can write

$$I_{D1} = I_{D2}$$

And from(c) and (d), we can write

$$I_{D3} = I_{D4}$$

Where, $K_n = 0.5\mu n C_{OX} W/L$ is transconductance parameter $V_{TN}$ is the threshold voltage of each n-channel MOSFET. And input biasing circuit voltage

$$V_1 = V_{c1} + \frac{1}{2} V_{34}$$

$$V_2 = V_{c1} + \frac{1}{2} V_{34}$$

This yields

$$\sqrt{V_{31}} \cdot \sqrt{V_{32}} = \sqrt{V_{12}} = \sqrt{V_{13}} = \sqrt{V_{14}}$$ \hspace{0.5cm} (7)

$$V_{34}$$ is also a differential input voltage with DC common mode $V_{c2}$.

Considering the output nodes, the differential output voltage is $V_{out} = V_{o1} - V_{o2}$. Where,

$$V_{o1} = V_c + (I_{D6} - I_{D2}) R$$ \hspace{0.5cm} (11a)

$$V_{o2} = V_c + (I_{D4} - I_{D3}) R$$ \hspace{0.5cm} (11b)

Where $V_c$ is reference common mode output voltage and $R$ are load resistors. Substituting (9) and (10) into (11) after subtracting

$$V_{out1} = 2R \sqrt{K_p (\sqrt{I_{D1}} - \sqrt{I_{D2}})} V_{id2} \hspace{0.5cm} (12)$$

At last, substituting (7) into (12) so

$$V_{out} = 2R \sqrt{K_n \cdot K_p} V_{id1} V_{id2}$$

Thus voltage gain can be adjusted by the load resistor and transconductance parameters.

VI. Simulation Results

To verify the operation of the circuits, the designs are simulated using ELDO tool (Mentor Graphics) for 0.18µm tsmc
CMOS technology. The aspect ratio of transistors and selected design parameters are shown in Table 1,2 and Table 3. The voltage supplies are set to at Vdd = 0.9v and Vss = 0v.

**TABLE I**
Aspect ratio of Transistor of FVF cell

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W(µM)</th>
<th>L(µM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>110</td>
<td>2</td>
</tr>
<tr>
<td>M2</td>
<td>17.8</td>
<td>2</td>
</tr>
<tr>
<td>M3</td>
<td>0.5</td>
<td>0.5</td>
</tr>
</tbody>
</table>

**TABLE II**
Aspect ratio of Transistor of Multiplier based on FVF cell

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W(µm)</th>
<th>L(µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 - M4</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>M5, M6, M8, M9</td>
<td>17.8</td>
<td>2</td>
</tr>
<tr>
<td>M7, M10</td>
<td>110</td>
<td>2</td>
</tr>
</tbody>
</table>

**TABLE III**
Various parameter of multiplier based on FVF cell

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1 = R2 = R3= R4</td>
<td>4KHz</td>
</tr>
<tr>
<td>VC</td>
<td>0.35v</td>
</tr>
<tr>
<td>VC1</td>
<td>0.70v</td>
</tr>
<tr>
<td>VC2</td>
<td>0.12v</td>
</tr>
</tbody>
</table>

The DC-transfer characteristic of the fvf cell is shown in Fig.4, when Vb varied from -0.4v to 0.4v with increment of 0.1v and Vb = 0.7v. Also shown Transient response in Fig 5 & Frequency Response in Fig 6.

**Fig.4** DC Response of FVF cell circuit

**Fig.5** Transient Response of FVF cell circuit

The DC-transfer characteristic of the multiplier based on fvf cell is shown in Fig.7, when V12 is input voltage varied from -0.1v to 0.1v with increment of 0.01v and V34 is varied from -0.08v to 0.08v with increment of 0.1v.

**Fig.6** Frequency response of FVF Cell

**Fig.7** DC-transfer characteristic of the multiplier based on fvf

**Fig.8(a)** V12 carrier sinusoidal signal (b) V34 sinusoidal signal (c) transient response of multiplier

**Fig.8** Frequency response Vo/V34 of the multiplier based on fvf

A multiplier circuit using the flipped voltage follower cell is presented with advantages of simple structure, few devices,
wide dynamic input range and low voltage supply. Simulation results prove that all circuits can operate at ±0.9V power supplies. So its compact structure makes it suitable for use in analog VLSI system.

REFERENCES