Research Paper Engineering

Four- quadrant Analog Multiplier Based on a Flipped Voltage Follower Cell in 0.18µm CMOS Technology

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ABSTRACT

In this paper CMOS voltage mode four quadrant analog multiplier circuit is proposed. It is based on FVF cell. The multiplier combines the features of both, the Flipped voltage follower cell and Square rooting circuit. The circuit is designed and analyzed in 0.18µm CMOS process model and simulation results have shown that, under single 0.9V supply voltage, and it consumes only 29µw quiescent power.

Keywords : analog multiplier, four-quadrant, flipped voltage follower, square rooting circuit

I. INTRODUCTION

Multiplier is an essential part for many analog applications. The multiplier performs a linear product of continuous signals x and y yielding an output z = Kxy, where K is a constant with suitable dimension. Varieties of multipliers have been designed for different optimization objectives [1][6].It is used in many applications such as voltage-controlled amplifier, ring modulator, product detector, frequency mixer, companding, squelch, analog computer, analog signal processing, automatic gain control, true RMS converter, analog filters. These applications are required to operate in low voltage environment for improving their power efficiency and incorporating with mixed signal systems to be used in portable application. There are classified in several types of analog multipliers namely, single quadrant analog multiplier, two quadrant analog multiplier and four quadrant analog multiplier. A four quadrant multiplier is one where inputs and outputs may swing positive and negative, while two-quadrant multiplier only has one input that has one polarity. Besides that, single quadrant analog multiplier only has inputs and outputs with only one polarity. To implement the multipliers in IC technologies, the Gilbert cell is a popular and oldest structure in IC technologies due to wide dynamic range and high frequencies performance. In CMOS technology, approaches which are important for most applications are CMOS multipliers using MOS transistors working in saturation region, and non-saturation region [8].

In this paper, we proposed a CMOS analog multiplier classified as Type IV, which has single low supply voltage, and is compatible with low-power operation. In order

to get a lower power supply and power consumption, concentrating on circuit topologies, which circuit cell called “flipped voltage followers”(FVF). It has been used for design since it needs only a supply voltage of VTH – Veff , where VTH is the threshold voltage and Veff(=VGS – VTH) is the effective gate voltage.

The paper is divided into four sections. Second section discusses the basics of multiplier operation and overview of Flipped voltage follower and Square rooting circuit .Third section includes how to design the Multiplier based on FVF cell circuit. In fourth section, simulation results are presented. In fifth section, conclusion regarding the multiplier is discussed.

II. PRINCIPLE OF OPERATION

In order to make a new circuit design, MOS Transistor is an important piece of device used in this study. By using drain circuit equation of MOS Transistor which works on saturated range. There are two styles of a squaring circuit and both of them work on the basic of the same principle. The relationship of the drain current is given by:

ID = KN(VGS – VTN)2 ; VGS > VTN , VDS ≥ VGS – VTN (1)
ID = KP(VGS – VTP)2 ; VGS > VTP , VDS ≥ VGS – VTP (2)

Where, KN and KP are the transconductance parameter of NMOS and PMOS, respectively VTN and VTP are the threshold voltages of NMOS and PMOS, respectively. VGS and VDS are the gate-to source voltage and the drain-to source voltage, respectively.

III. Flipped voltage follower cell

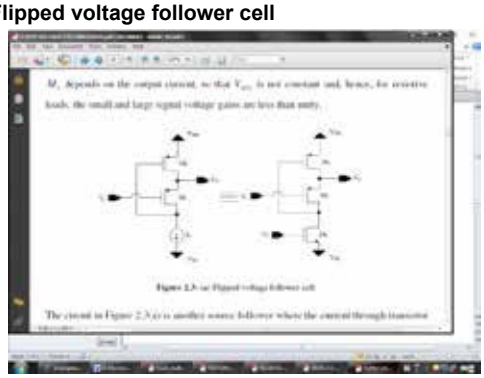

Fig. 1 Filpped voltage follower cell[4]

The circuit in Fig. 1 is source follower where the current through transistor M1 is held constant,and not depend on the output current. It could be described as a voltage follower with shunt feedback. Neglecting body effect and the short-channel effect, VGSM1 is held constant, and voltage gain is unity. Circuit is able to source a large amount of current, but its sinking capability is limited b the biasing current source Ib , due to the low impedance at the output node,

$$R_O = \frac{1}{g_{m1} g_{m2} \cdot r_{O1}} \quad (3)$$

Where , gmi and gm2 are the transconductance of the transistor M1 and M2 respectively, and roi is the output resistance

The equation (3) shows that the circuit has very low output resistance usually required for voltage source. This value is in the order of 20-100 Ohms. The relationship of the voltage at the terminal Vo to bias current of M3.

2) .Square rooting circuit

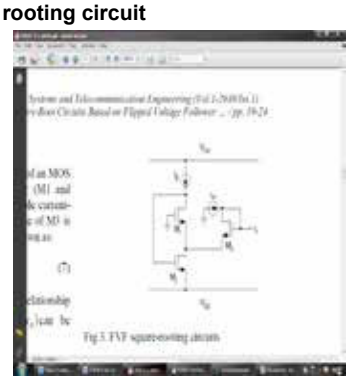

Fig. 2 FVF square-rooting circuits[3]

The square-rooting circuit shown in Fig.2 consists of an MOS transistor (M3) and the flipped voltage follower (M1 and M2). The transistor M3 in fig.3 is used as a simple current to-voltage converter. When source terminal voltage of M3 is equal to -VTN therefore, the current of equation shown as:

$I_{in} = I_D3$ (4)

When $I_{D3} = K_N(VO – (-V_{TN}) – V_{TN})^2 = K_N VO^2$ .The relationship

between input current (I_{in}) and output voltage (V^o) can be expressed as:

(5) $V_o = \sqrt{Iin/kn}$

V. circuit design

Fig.3 shows the circuit of four quadrant analog multiplier based on FVF cell consisting of combination of common source amplifier with a differential voltage controlled square rooting circuit.

The multiplier circuit formed by common source amplifiers M1-M4 connected pair of differential flipped voltage followers (DFVF). M5-M7and M8 – M10. All transistor work on saturation region, the drain currents of M1 to M4 are given as:

$ID1 = K_n(V1 – V_{tn})^2$ (6.a)

$ID2 = K_n(V1 – V_{tn})^2$ (6.b)

$ID3 = K_n(V2 – V_{tn})^2$ (6.c)

$ID4 = K_n(V2 – V_{tn})^2$ (6.d)

From (a) and (b), we can write

$I_D1 = I_D2$

And from(c) and (d), we can write

$I_D3 = I_D4$

Where, Kn = 0.5μn Cox W/L is transconductance parameter Vtn is the threshold voltage of each n-channel MOSFET. And input biasing circuit voltage

$V_1 = V_{c1} + 1/2\ V_{12}$,

$V_2 = V_{c1} + 1/2\ V_{12}$.,

This yields

$\sqrt{I_{D1}} - \sqrt{I_{D4}} = \sqrt{I_{D2}} - \sqrt{I_{D3}} = \sqrt{K_n}\, V_{12}$ (7)

Where V12 is differential input voltage with DC common mode Vc1.The nonlinear relation can be removed by injecting the output current into square-rooting circuit, which ID1 is injected from bias current of the differential-FVF(DFVF). Similarly, the bias current of the circuit M8-M10 is obtained by injecting ID4 into the M8. This results in ID5 = ID4 and ID8 = ID4.

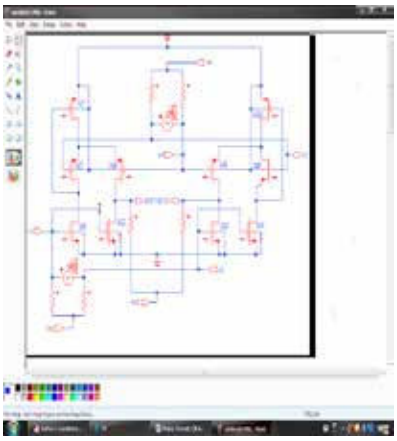

Fig.3 Multiplier based on FVF cell circuit

Now focus on the voltage controlled square-rooting circuit. From Fig.3 we observe that

$V_3 - V_4 = V_{SG6} – V_{SG5} = V_{SG8} – V_{SG7}$ (8)

By applying the square law relation of a p-channel MOSFET so drain current is :

$I_D = K_p(V_{SG} – |V_{tp}|)2$

And input biasing circuit voltage

$V_3 = V_{c2} + 0.5\ V_{34}$,

$V_4 = V_{c2} + 0.5\ V_{34}$,

we get :

$$I_{D6} = K_p \left(V_{id2} + \sqrt{\frac{I_{D1}}{K_p}}\right)^2 \quad (9)$$

$$I_{D8} = K_p \left(V_{id2} + \sqrt{\frac{I_{D1}}{K_p}}\right)^2 \quad (10)$$

Where V34 is also a differential input voltage with DC Common mode Vc2 .
Considering the output nodes, the differential output voltage is Vout = Vo1 – Vo2. Where,

$V_{o1} = V_c + (I_{D6} – I_{D2})\ R$ (11a)

$V_{o2} = V_c + (I_{D8} – I_{D3})\ R$ (11b)

Where Vc is reference common mode output voltage and R are load resisters. Substituting (9) and (10) into (11) after subtracting

$$V_{out} = 2R\sqrt{K_P}\left(\sqrt{I_{D1}} - \sqrt{I_{D4}}\right)V_{id2} \quad (12)$$

At last, substituting (7) into (12) so

$$V_{out} = 2R\sqrt{K_n}\, K_p V_{id1} V_{id2}$$

Thus voltage gain can be adjusted by the load resistor and transconductance parameters.

VI. Simulation Results

To verify the operation of the circuits, the designs are simulated using ELDO tool (Mentor Graphics) for 0.18μm tsmc

CMOS technology. The aspect ratio of transistors and selected design parameters are shown in Table 1&2 and Table 3. The voltage supplies are set to at Vdd = 0.9v and Vss = 0v.

TABLE I
Aspect ratio of Transistor of FVF cell

Transistor	W(μM)	L((μM)
M1	110	2
M2	17.8	2
M3	0.5	0.5

TABLE II
Aspect ratio of Transistor of Multiplier based on FVF cell

Transistor	W(μm)	L(μm)
M1- M4	0.5	0.5
M5,M6,M8,M9	17.8	2
M7,M10	110	2

TABLE III
Various parameter of multiplier based on FVF cell

Parameter	Values
R1 = R2 = R3= R4	4KHz
VC	0.35v
VC1	0.70v
VC2	0.12v

The DC-transfer characteristic of the fvf cell is shown in Fig.4, The input voltage Vb varied from -0.4v to 0.4v with increment of 0.1v and Vb = 0.7v. Also shown Transient response in Fig 5 & Frequency Response in Fig 6.

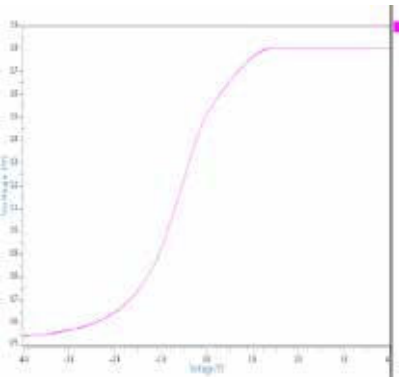

Fig.4 DC Response of FVF cell circuit

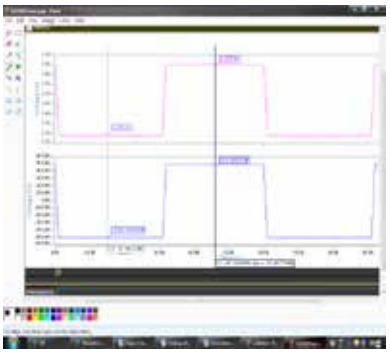

Fig.5 Transient Response of FVF cell circuit

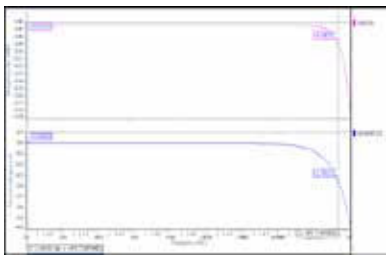

Fig.6 Frequency response of FVF Cell

The DC-transfer characteristic of the multiplier based on fvf cell is shown in Fig.7, when V12 is input voltage varied from -0.1v to 0.1v with increment of 0.01v and V34 is varied from -0.08v to 0.08v with increment of 0.1v.

Fig. 8 shows the application of the four quadrant multiplier as a balance modulator. The modulation is performed when the input voltage is 0.6v, 300MHz sinusoidal Vid1 is a carrier signal multiplied with another signal voltage is 0.6v,25 MHZ sinusoidal Vid2 is modulated signal.

Frequency response of the multiplier topology is shown in Fig. 9. Here the output voltage Vo versus the input voltage V12. The -3db bandwidth is about 10MHz.

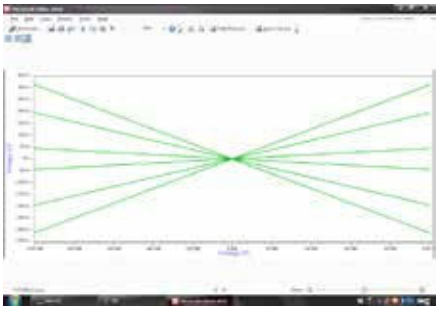

Fig.7 DC-transfer characteristic of the multiplier based on fvf

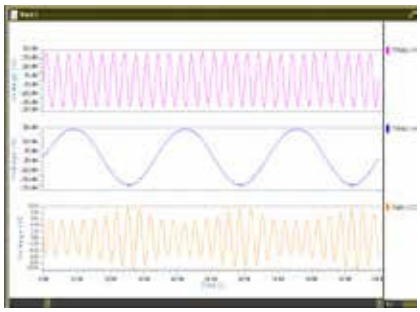

Fig.8(a) V12 carrier sinusoidal signal (b) V34 sinusoidal signal(c)transient response of multiplier

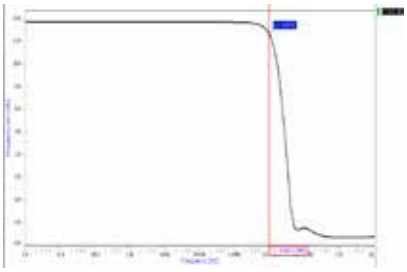

Fig.9 Frequency response Vo/V34 of the multiplier based on fvf

VII. Conclusion
A multiplier circuit using the flipped voltage follower cell is presented with advantages of simple structure, few devices,

wide dynamic input range and low voltage supply. Simulation results prove that all circuits can operate at ±0.9V power supplies. So its compact structure makes it suitable for use in analog VLSI system.

REFERENCES

C. Chen, Z. Li., "A Low Power CMOS Analog Multiplie,"IEEE Transactions on Circuits and Systems .11, Volume 53, pp. 100-104, Feb. 2006. | N. Kiatwarin, W. Ngamkham and W. Kiranon "A Compact Low Voltage CMOS Four-QuadrantAnalog Multiplier" ECTI International Conference App 2007 | Chaiwat Sakul , Kobchai Dejhan" Squaring And Square-Root Circuits Based On Flipped Voltage Follower And Applications" International Journal of Information Systems and Telecommunication Engineering (Vol.1-2010/Iss.1) pp 19-24 App.2010. | Neeraj Yadav 1, Sanjeev Agrawal 2, Jayesh Rawat 3, Chandan Kumar Jha "Low Voltage Analog Circuit Design Based on the Flipped Voltage Follower "International Journal of Electronics and Computer Science Engineering ISSN: 2277-1956 pp 258-273 | Amir h. Miremadi , Ahmad Ayatollahi ,Amir H. Miremadi," A Low Voltage Low Power CMOS Analog Multiplier" IEEE App.2011. | Ramraj Gottiparthy" AN ACCURATE CMOS FOUR-QUADRANT ANALOG MULTIPLIER" ,Master of Science thesis, Department of Electrical and Computer Engineering ,Auburn University 2006 | Amit Chaudhary "Low Voltage Analog Circuits Based on Flipped Voltage Follower cell", M.Tech thesis , Dept. of electronics & communication, Thaper University 2010. | Baker, Li, Boyce 1997. CMOS: Circuit Design, Layout and Simulation 2nd ed. New York: John Wiley & Sons. 1997 .