Research Paper Engineering

# Design and Analysis of low power 8T SRAM

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**ABSTRACT**

*A SRAM cell must meet requirements for operation in submicron/nano ranges. The scaling of CMOS technology has significant impact on SRAM cell -- random fluctuation of electrical characteristics and substantial leakage current. In this paper we present dynamic column based power supply 8T SRAM cell and comparing the proposed SRAM cell with respect to conventional SRAM 6T in respect to power and delay. Simulation results affirmed that proposed 8T SRAM cell consumes less power as compare to basic 6T SRAM cell with improved read stability, read current, and leakage current on different technologies.*

**Keywords: Kanban, lean, Takt, WIP, Through-Put-Time, SWOT analysis, Build-to-Order.**

**1. INTRODUCTION**

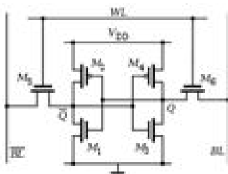
For nearly 40 years CMOS devices have been scaled down in order to achieve higher speed, performance and lower power consumption. Static Random Access Memory (SRAM) continues to be one of the most fundamental and vitally important memory technologies today. As process technology is scaled down, threshold voltage and leakage current variations are increased [1]. In the conventional 6T cell, it is difficult to find an optimum design because the both read stability and write margin must be considered. At low supply voltage 6T cell worsen in read stability. Leakage power is a high priority consideration due to feature scaling in high performance processor design. In today's processors, the leakage power of cache was a major source of power dissipation because cache occupies more than 50% of the chip area [2]. Low leakage SRAM design leakage SRAM design has been an active area of research over the past years. Low Power and high-stability have been the main themes of SRAM designs in the last decade [8].In this paper, we use dynamic cell supply 8T SRAM cell to address the above problems. We compare the conventional 6T and proposed 8T SRAM cell with respect to read stability and leakage.

Section 2 reviews the basic operation of conventional 6T SRAM cell. Section 3 presents the operating principles of proposed cell and its circuit implementation. Section 4 presents Schematic view of conventional 6T and 8T on mentor Graphics EDA Tool. Section 5 presents simulation results. Section 6 represent conclusion of the paper.

**2. CONVENTIONAL 6T SRAM CELL**

**2.1 CONSTRUCTION**

Fig 1 shows the conventional 6T SRAM cell which has two back to back connection of inverters using N1, P1, N2, P2 to store the single bit either '0' or '1'. N3, N4 transistors are called as access transistors. WL is used to turn ON the access transistors. BL, /BL are bit lines.



Conventional 6T SRAM Cell

**2.2 OPERATION**

An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows [5] [7]:

**Standby**: If the word line is not asserted, the access transistors N3 and N4 disconnect the cell from the bit lines. The two cross coupled inverters formed by P1-N1, P2-N2 will continue to reinforce each other as long as they are connected to the supply.

• **Reading:** Assume that the content of the memory is a 1, stored at D. The read operation is done by using the sense amplifiers that pull the data and produce the output. The row decoders and column decoders are used to select the appropriate cell or cells from which the data is to be read and are given to the sense amplifiers through transmission gate.

• **Writing:** The start of a write cycle begins by applying the value to be written to the bit

lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL bar to 1 and BL to 0. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters.

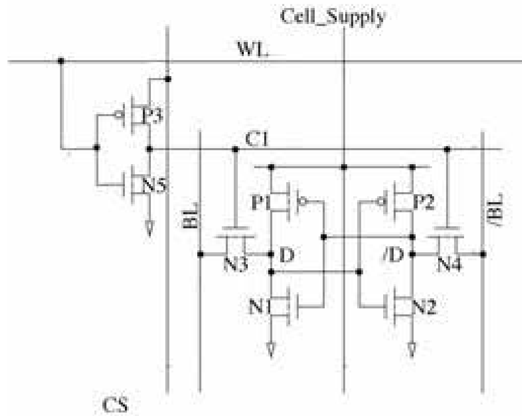
**3. PROPOSED 8T SRAM CELL**

**3.1 CONSTRUCTION**

The proposed SRAM cell consists of 8 transistors, N1-N5 and P1-P3, as shown

Fig.4. Four transistors N1, N2, P1, P2 form a cross-couple structure to store data. Four transistors P3 and N3- N5 are access to the internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes D and /D of the cell. N3 and

N4 connect the cell internal nodes to the BLs while P3 and N5 form an inverter to control the voltage of node C1. The source terminal of P3 is connected to a column select (CS) line while gates of P3 and N5 are connected to WL. Unlike conventional design, the sources of P1 and P2 are connected to dynamic cell supply(*cell_supply*) line which is raised to the higher voltage during read operation to obtain a higher noise margin [4].




Newly design 8T SRAM cell

### 3.2 OPERATION

Like a conventional 6T SRAM bit cell, it has three modes of operations*: standby read and write* as follows [4]:

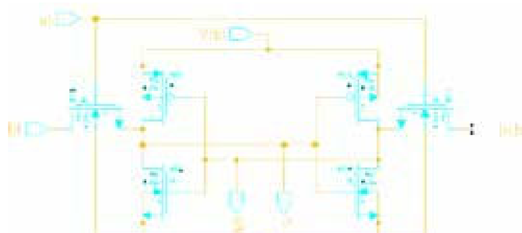
**Standby:** During standby, *Cell_Supply* voltage is kept at VDD to maintain a high noise margin. at the same time WL is pre-charged high while all CS is pre-charged low. As a result, transistor N5 of cell is turned on to pre-charge node C1 to ground. Thus, both access transistors N3 and N4 turned off, isolating the storing element from any BL disturbances. Also, BLs are pre-charged to VDD to prepare for the next read/ write operation.

**Reading:** A read operation start by raising CS from ground to VDD and Cell_Supply is raised from VDD to VDD2. VDD2 must be higher than VDD to improve noise margin of cell during read operation. At the same time WL is pulled to low to drive node C1 to VDD and hence turning on N3 and N4. Once N3 and N4 are turned on to read the cell data, subsequent circuit operation same as the conventional 6T SRAM.

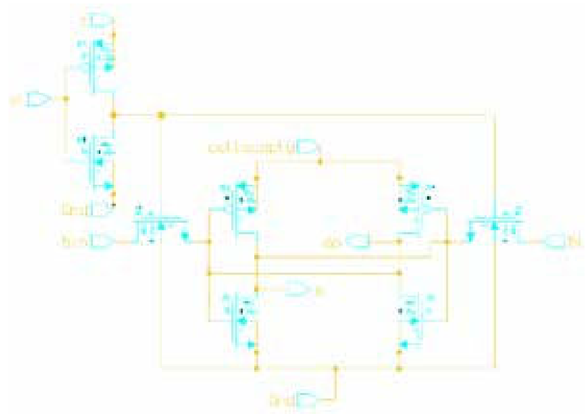
**Writing:** Write operation of the proposed design is much simpler than its read operation. Write operation starts by asserting CS line to VDD while the WL is pulled down. Meanwhile, one of the BLs is pulled to ground while other kept at VDD. When node C1 is charged up to VDD, both N1 and N2 are turned on and input data is written into memory similar to conventional 6T SRAM.

### 4. Schematic view

Using Mentor Graphics EDA Tool we have design of both conventional and proposed system on schematic window. Fig 6 & Fig 7 shows the schematic for conventional 6T and proposed 8T using schematic editor. After that we have analyze them on different process technology i.e. on 180nm, 250nm, 350nm and 500nm create symbols for both and analysis those cells in respect to average power consumption and delay.



Schematic view of 6T SRAM cell



Schematic view of newly design 8T SRAM cell

### 5. Simulation Result

With the help of mentor graphics we have analyze them on the basic of power consumption and delay on different technologies i.e. at 180nm, 250nm, 350nm and 500nm as shown in table

**6-transistor SRAM**

| L | Supply Voltage | Power consumption | Delay | Power Delay Product |
|---|---|---|---|---|
| 180nm | 1.2v | 0.724 mw | 0.2596ns | 0.1879 |
| | 1.5v | 0.809 mw | 0.2645ns | 0.2139 |
| | 1.8v | 0.8872mw | 0.2780ns | 0.2466 |
| 250nm | 1.2v | 0.745mw | 0.2912ns | 0.2169 |
| | 1.5v | 0.823mw | 0.2994ns | 0.2464 |
| | 1.8v | 0.959mw | 0.3017ns | 0.2893 |
| 350nm | 1.2v | 0.761mw | 0.3319ns | 0.2525 |
| | 1.5v | 0.835mw | 0.3534ns | 0.2950 |
| | 1.8v | 1.0397mw | 0.3967ns | 0.4124 |
| 500nm | 1.2v | 0.817mw | 0.4389ns | 0.3699 |
| | 1.5v | 0.986mw | 0.4679ns | 0.4613 |
| | 1.8v | 1.1435mw | 0.5146ns | 0.5884 |

**8-transistor SRAM**

| L | Supply Voltage | Power con sumption | Delay | Power Delay Product |
|---|---|---|---|---|
| 180nm | 1.2v | 0.687 mw | 0.2612ns | 0.1795 |
| | 1.5v | 0.777mw | 0.2669ns | 0.2074 |
| | 1.8v | 0.854mw | 0.2689ns | 0.2297 |
| 250nm | 1.2v | 0.7231mw | 0.2747ns | 0.1987 |
| | 1.5v | 0.818mw | 0.2766ns | 0.2263 |
| | 1.8v | 0.8928mw | 0.2971ns | 0.2653 |
| 350nm | 1.2v | 0.7301mw | 0.3281ns | 0.2396 |
| | 1.5v | 0.817mw | 0.3357ns | 0.2743 |
| | 1.8v | 0.969mw | 0.3919ns | 0.3798 |
| 500nm | 1.2v | 0.8010mw | 0.4387ns | 0.3514 |
| | 1.5v | 0.9374mw | 0.4388ns | 0.4114 |
| | 1.8v | 1.067mw | 0.5009ns | 0.5345 |

### 7. CONCLUSION

A fully differential 8T SRAM with a column-based dynamic supply has been proposed. Analyze both conventional 6T and proposed SRAM based on power consumption and delay. The proposed SRAM 8T cell has achieved improved read stability, read current and leakage current. From the above results it has been seen that power consumption in newly de-

sign 8T SRAM is reduced up to 8 to 22 % but correspondingly delay is increases up to 4 to 8.5% this is clearly visualize in the power delay product that the PDP of 8T SRAM is better than 6T Conventional SRAM up to 3 to 11 %.

## REFERENCES

[1]K. Dhanumjaya1, m. Sudha2, dr.mn.giri prasad3, dr.k.padmaraju4 "cell stability analysis of conventional 6t dynamic 8t sram cell in 45nm Technology" (vlsics) vol.3, no.2, vlsic.2012.3204 41-51 | [2] V. Gupta and M. Anis, "Statistical design of the 6T SRAM bit cell," IEEE Trans. Circuits Syst. I,Reg. Papers, vol. 57, no. 1, pp. 93–104, Mar. 2010. | [3] C. Molina, C. Aliagas, M. Garcia, A. Gonzcalezo, J. Tubellao. Non Redundant Data Cache. In ISLPED, pages 274–277, August 2003. | [4] E. Grossar et al., "Read stability and write-ability analysis of SRAM cells for nanometer technologies," IEEE J. Solid-State Circuits, vol.41, no. 11, pp. 2577–2588, Nov. 2006. | [5] Do Anh-Tuan, Jeremy Yung Shern Low, Joshua Yung Lih Low, Zhi-Hui Kong, Xiaoliang Tan, and Kiat-Seng Yeo,"An 8T Differential SRAM With Improved Noise Margin for Bit-Interleaving in 65 nm CMOS" IEEE Transnctions on circuits and systems—I :regular papers, Vol. 58, No. 6, june 2011. | [6] Jan M. Rabaey,Anantha Chandrakasan and Borivoje Nikolic, "Digital Integrated Circuits", ISBN 81-7808-991-2, Pearson Education, 2003. | [7] Antonio J. Lopez Martin"CADENCE DESIGN ENVIRONMENT"Klipsch School of Electrical and Computer Engineering, New Mexico State University, October 2002. | [8] Neil H.E.Weste,David Harris and Ayan Banerjee, "CMOS VLSI Design, a circuits and systems perspective" ,ISBN: 0321149017/9780321 149015 Third edition, Pearson Education, 2005. | [9] C. Ik Joon et al., "A 32 kb 10T sub threshold SRAM array with bit inter leaving and differential read scheme in 90 nm CMOS," IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 650–658, Feb. 2009. | [10] E. Seevinck et al., "Static-noise margin analysis of MOS SRAM cells," IEEE J. Solid-State Circuits, vol. SSC-22, no. 5, pp. 748–754, Oct.1987.