Research Paper Engineering

Design of Highly Linear CMOS Gm-Cell for Continuous time filter Applications

* Pramod Kumar Jain ** D. S. Ajnar
*** Pankaj Naik

* Department of Electronics and Instrumentation, SGSITS Indore, India

** Department of Electronics and Instrumentation, SGSITS Indore, India

*** Department of Electronics and Instrumentation, SGSITS Indore, India

ABSTRACT

In this paper, a linearity improvement technique is proposed for a low-distortion filter operating in high frequency ranges. The proposed transconductor eliminates value at the output by superposing the opposite non-linear behaviors of two differential structures in parallel.

Keywords: Low-distortion transconductor, linearization technique, Gm-C filter, flat band-pass.

I.INTRODUCTION

HIGH-FREQUENCY

low-distortion continuous-time filters have many applications in the radio and video frequency filtering sections of communication transceivers.

There are various filter types that are appropriate for the implementation of on-chip continuous time filters. Those are active-RC filters, switched-capacitor filters and Gm-C filters. Though high linearity is an advantage of both active-RC and switched-capacitor filters, these filters have a disadvantage of operating at high frequency ranges due to the limitation of the unity bandwidth of the operational amplifier (OPAMP). Besides, it is not easy to implement tuning scheme for those two filter types. Meanwhile, G_m-C filters are popular for on-chip applications due to their advantages of high frequency performance and low power consumption, but have linearity problems. In order to overcome the disadvantage of linearity of G_m-C filters, many linearization techniques for transconductor have been reported. Fig. 1 shows some well-known linearization techniques. The resistive source degeneration technique shown in Fig. 1(a) may be the simplest and most well-known one, in which the linearization is achieved at the cost of power consumption. Fig. 1(b) shows the dynamic source degeneration technique [1], which is an improved version of the structure shown in Fig. 1(a). Though the range of input signal levels that the transconductor is linear is broadened, the ripple of the G_m response over the input amplitude is still high. The tunable feedback technique [2] shown in Fig. 1(c) and its combination with the dynamic source degeneration technique [3] shown in Fig. 1(d) are also reported to achieve high linearity at the cost of high power consumption due to the additional bias feedback part. Fig. 1(e) shows a transconductor with bias feedback technique [4], in which the four additional transistors M_3, M_4, M_5 and M6 compose the adaptive biasing block besides the normal differential pair composed of two transistors and M_2. The additional block takes a role to keep the total current flowing through the main differential pair M_1 and M_2 balanced, increasing the linearity of the transconductor. Yet the obligated usage of a current tail in this bias feedback method limits its performance at low supply voltages. Besides, the technique is significantly affected by mismatching between the main differential pair and the adaptive biasing block.

II. TRANSCONDUCTOR DESCRIPTION

Fig. 3 shows the core structure schematic of a linearity improvement technique for the G_m-cell. In Fig. 4, there are

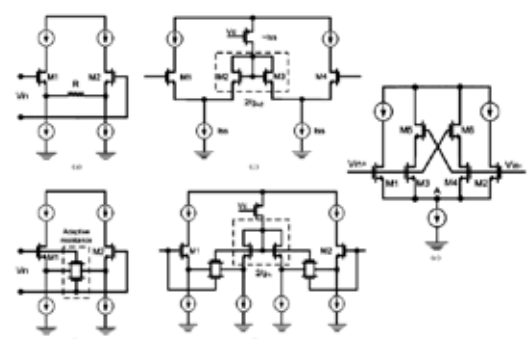


Fig. 1. Linearization techniques for Gm cells: (a) resistive source degeneration technique; (b) dynamic source degeneration technique; (c) tunable-feedback tech- nique; (d) source-degeneration tunable-feedback combined technique; (e) bias feedback (or adaptive biasing) technique.

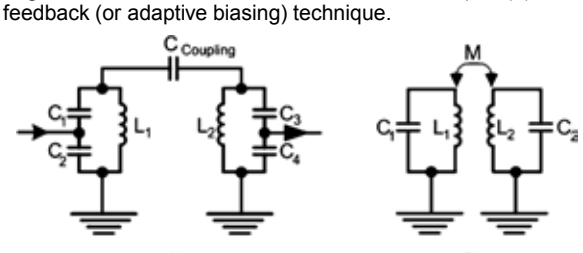


Fig. 2. Methods for making pass-band flat: (a) C-coupling method; (b) magnetic-coupling method

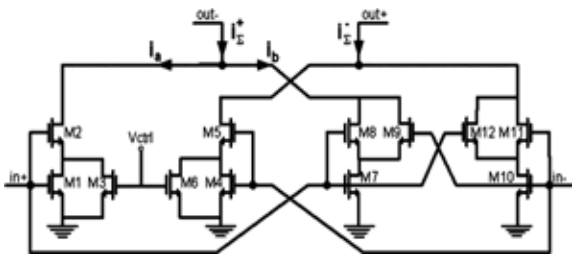
12 nMOS transistors M_1-M_{12}, of which two groups of nMOS transistors are categorized for the two sides of the structure.

The left wing of the structure is composed of nMOS transistors M_1-M_6 while the right wing is made of nMOS transistors M_7-M_{12} . In Fig.3, both the right and the left wings are in

differential structure. It means that there are pairs (M_1-M_4), (M_3-M_6), (M_2-M_5), (M_7-M_{10}), (M_8-M_{11}) and (M_9-M_{12}), in each of which, transistors are identical. From above descriptions, the proposed linearization method is analyzed based on the superposition of two paralleled differential structures with opposite behaviors of nonlinearity. These two opposite responses of the two parallel wings in Fig. 4 compensate one another to diminish non-linear elements. Therefore, the total distortion at the output of the G_m-cell can be reduced. The structure of the two parallel sides, which are explained above is pseudo differential which is more suitable for low voltage design. Fig. 4(a) and (b) show the halves of circuits in the left and the right wings described in Fig. 4, respectively. The both half circuits shown in Fig. 4(a) and (b) share the same self-cascode structure part, which is composed of transistors M_1 and M_2 in Fig. 4(a), and transistors M_7 and M_8 in Fig. 4(b). Based on the characteristics of self-cascode circuit, it can be realized that M_1 and M_7 operate in triode region while and are in saturation region. From Fig. 4(a).

$$i_2 = k_2(V_{cm} + v - V_x - V_t)^2 \quad (1)$$

$$i_1 + i_3 = k_1[2(V_{cm} + v - V_t)V_x - V_x^2] + k_3[2(V_c - V_t)V_x - V_x^2] \quad (2)$$



Where i_1 , $i_2$and $i_3$are the drain currents of transistors M_1, M_2 and M_3 respectively. V_{CM} and $\pm v$ are the common mode and small AC voltages of the input node, respectively. Vt is the threshold voltage of nMOS transistors, Vx is the voltage value at node X of Fig. 4(a), $k_i = \left(\frac{W}{L}\right)_i C_{ox}, (i = 1,2,3 \ldots 12), k_{ij} = k_i + k_j (i \neq j)$ and $k_{ij} = k_i + k_j + k_l (i \neq j \neq l)$. In Fig. 5, V_{CM} + v is applied at the inputs of transistors M_1, M_2, M_7 and M_8, while V_{CM} - v is at the input of M_2 in Fig. 4(b).

Since $i_2 = i_1 + i_3$ from (1) and (2), the voltage of node X can be expressed as

$$V_x = V_{CM} - V_t + \frac{k_{12}v - \sqrt{\Delta_x'}}{k_{123}}$$

Where

$$\Delta_x' = (k_{12}^2 - k_{123}k_2)v^2 + 2k_{123}k_1(V_{CM} - V_t)v + k_{123}k_{13}(V_{CM} - V_t)^2 \quad (4)$$

Therefore from (1) and (3), the drain current ia shown in fig 4(a) can be given by

$$i_a = i_2 = k_2\left(\frac{k_2 v + \sqrt{\Delta_x'}}{k_{123}}\right)^2 \quad (5)$$

Similarly, the drain current ib shown in Fig. 4(b) can be given by

$$i_b = i_7 = k_8\left(\frac{2k_9 v + \sqrt{\nabla_y'}}{k_{789}}\right)^2 + k_9\left(\frac{-2k_7 v + \sqrt{\Delta_y'}}{k_{789}}\right)^2 \quad (6)$$

where i_7, i_8 and i_9 are the drain currents of transistors M_7, M_8 and M_9, respectively; and

$$\Delta_y' = [(k_7 - k_9)^2 - k_{789}k_{89}]v^2 + 2k_{789}k_7(V_{CM} - V_t)v + k_{789}k_7(V_{CM} - V_t)^2 \quad (7)$$

Thus, from (5) and (6), the total drain current in Fig. 3 can be given as

Thus, from (5) and (6), the total drain current $i_\Sigma^+ i_\Sigma^-$ in Fig. 3 can be given as

Since the proposed transconductor is as differential structure as shown in Fig. 3, from (8), the differential output current of the transconductor is

$$= \frac{k_2}{k_{123}^2}\Delta_x' + \frac{k_{89}}{k_{789}^2}\Delta_y' + \left[\frac{k_2 k_3^2}{k_{123}^2} + 4\frac{k_9 k_8^2 + k_9 k_7^2}{k_{789}^2}\right]v^2 + \left[\frac{2k_2 k_3}{k_{123}^2}\sqrt{\Delta_x'} - \frac{4k_{789}k_9}{k_{789}^2}\sqrt{\Delta_y'}\right]v \quad (8)$$

$$i_{out} = i_\Sigma^+ - i_\Sigma^- = \frac{k_2}{k_{123}^2}[\Delta_x'(v) - \Delta_x'(-v)] + \frac{k_{89}}{k_{789}^2}[\Delta_y' v(v) - \Delta_y'(-v)] + \left[\frac{2k_2 k_3}{k_{123}^2}\left(\sqrt{\Delta_x'(v)} + \sqrt{\Delta_x'(-v)}\right) - \frac{4k_{789}k_9}{k_{789}^2}\left(\sqrt{\Delta_y'(v)} + \sqrt{\Delta_y'(-v)}\right)\right]v \quad (9)$$

where, from (4) and (7),

$$\sqrt{\Delta_x'(v)} + \sqrt{\Delta_x'(-v)} = 4k_{123}k_1(V_{CM} - V_t)v \quad (10)$$

$$\sqrt{\Delta_y'(v)} + \sqrt{\Delta_y'(-v)} = 4k_{789}k_7(V_{CM} - V_t)v \quad (11)$$

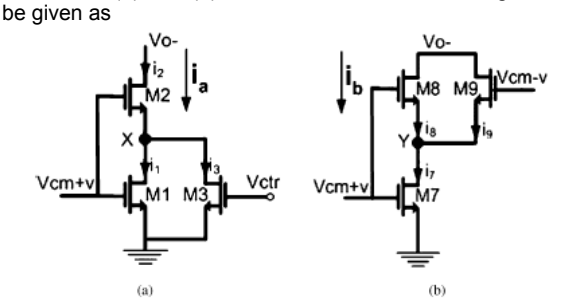


Fig. 4. The two half circuits of the two wings of Fig. 3, (a) the half of the left wing in Fig. 4, (b) the half of the right wing in Fig. 3.

tions (10) and (11) show that $\sqrt{\Delta_x'(v)} + \sqrt{\Delta_x'(-v)}, \sqrt{\Delta_x'(v)} + \sqrt{\Delta_x'(-v)}$ and $\sqrt{\Delta_y'(v)} + \sqrt{\Delta_y'(-v)}, \sqrt{\Delta_y'(v)} + \sqrt{\Delta_y'(-v)}$ are linear components. Thus, in (9) is the distortion source of the differential output current i_{out} . Because of the fact that (9) is the differential expression of (8), it is easy to recognize $\left[\frac{2k_2k_3}{k_{123}^2}\sqrt{\Delta_x'} - \frac{4k_{789}k_9}{k_{789}^2}\sqrt{\Delta_y'}\right]$ as the nonlinear part of the output current i_Σ in (8).

Since $\left[\frac{2k_2k_3}{k_{123}^2}\sqrt{\Delta_x'} - \frac{4k_{789}k_9}{k_{789}^2}\sqrt{\Delta_y'}\right]$ in (8) is the source of distortion of the proposed transconductor, the component $\frac{2k_2k_3}{k_{123}^2}\sqrt{\Delta_x'}$ is the nonlinear contributor of the left wing shown in Fig. 4(a), while $-\frac{4k_{789}k_9}{k_{789}^2}\sqrt{\Delta_y'}$ is the nonlinear contributor of the right wing shown in Fig. 4(b). These two nonlinear components are opposite in sign and tend to cancel each other. And the highest linearity of the transconductor is achieved as these two distortion components of the left and the right wings cancel completely one another. Because of the fact that tuning the values of $\frac{2k_2k_3}{k_{123}^2}\sqrt{\Delta_x'}$ and $-\frac{4k_{789}k_9}{k_{789}^2}\sqrt{\Delta_y'}$ is implemented by controlling the sizes of transistors, the optimum condition for linearity can be achieved by changing the size of transistors in the G_m-cell. As a result, the 2nd derivative value G_m'' of the overall transconductance value G_m can be kept nearly zero over a large range of input signal amplitude.

III. SIMULATION RESULTS

Fig. 5 shows the simulation results of transconductance values G_m and their second derivatives G_m''. Fig. 5(a) shows the simulated transconductance values g_m of the left and the right wings as well as the overall transconductor shown in Fig. 3. Fig. 5(b) shows the simulation results of the second derivative values g_m'' of the left wing, the right wing and the proposed transconductor G_m'' value of the overall transconductor is the combination g_m'' of values of the left and the right wings. In Fig. 5(b), it can be seen that the g_m'' values of the left and the right wings are in opposite signs. The total G_m'' value of the transconductor is kept nearly zero over a large range of input signal.

Fig. 8 shows the simulations of the G_m and G_m'' values of the proposed G_m -cell at different temperatures. In Fig. 8(a),

though G_m varies, the flatness of the G_m behaviors over the input signal range stays the same. In Fig. 8(b), there is no significant change in G_m'' values over the temperature variation. Thus, the linearity of the proposed transconductor is not significantly dependent on temperature variations. Besides, the variation of G_m values versus temperatures in Fig. 8(a) is due to the change in the threshold voltages of transistors, so causing the change of the bias current. Therefore, it can be explained that the variation of the width of the G_m'' curves in Fig. 8(b) is because of the change in bias current of the G_m -cell.

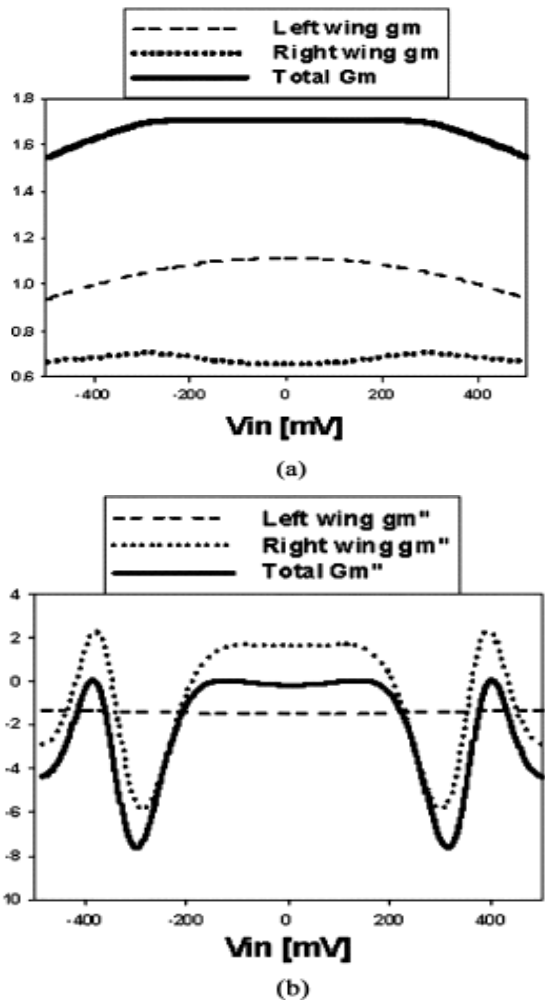


Fig. 5. Simulated characteristics of transconductances g_m and their derivatives

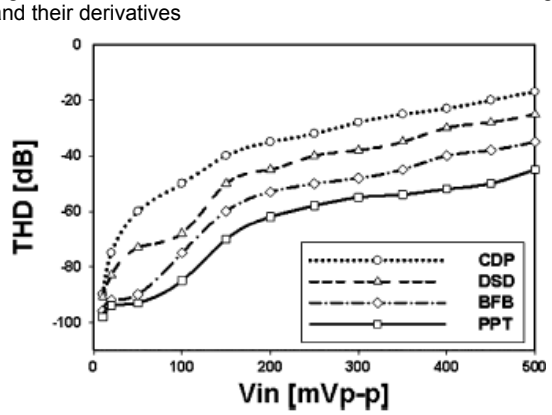


Fig. 6. Simulated total harmonic distortion (THD) versus the input voltage amplitudes for four cases of CDP, DSD, BFB, and PPT in the same voltage, current supplies and transistor channel length conditions.

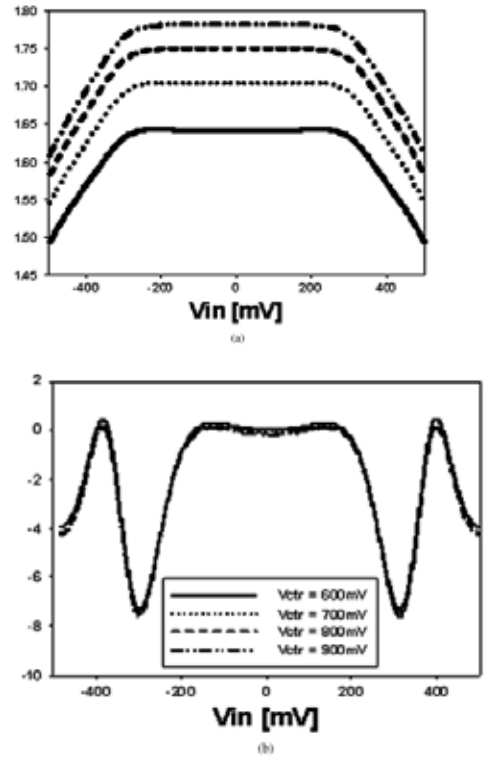


Fig. 7. The simulated variation of G_m'' value versus G_m tuning: (a) G_m tuning with control voltage from 600 mV to 900 mV; (b) the change of G_m'' versus G_m tuning.

IV. CONCLUSION

This paper has reported a linearization technique for transconductors used in a resonant-coupling filter. The proposed transconductor is suitable for high-frequency applications which require a low voltage supply and a large input range. The achieved results show the advantages of flat bandpass and stable ac shape of the resonant coupling structure.

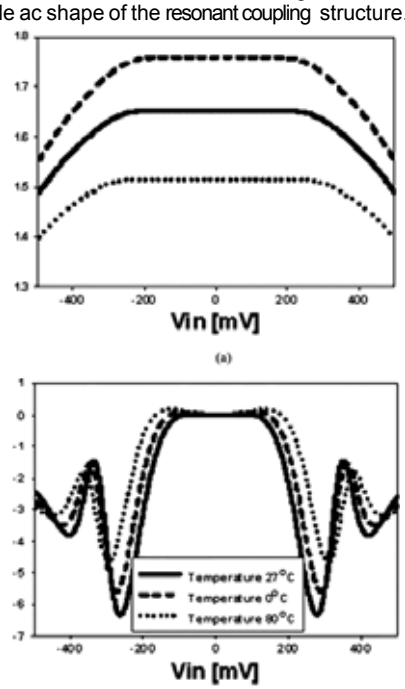


Fig. 8. The simulated variations of G_m and G_m'' versus temperature conditions:

(a) G_m variation; (b) G_m'' variation.

REFERENCES

[1] F. Krummenacher and N. Joehl, "A 4-MHz CMOS continuous-time filter with on-chip automatic tuning," IEEE J. Solid-State Circuits, vol. SC-22, no. 3, pp. 335–342, Jun. 1988. | [2] R. Torrance, T. Viswanathan, and J. Hanson, "CMOS voltage to current transducers," IEEE Trans. Circuits Syst., vol. CAS-32, no. 11, pp. 1097–1104, Nov. 1985. | [3] J. Silva-Martinez, M. S. J. Steyaert, and W. M. C. Sansen, "A large-signal very low-distortion transconductor for high-frequency continuous-time filters," IEEE J. Solid-State Circuits, vol. 26, no. 7, pp. 946–955, Jul. 1991. | [4] C. S. Kim, Y. H. Kim, and S. B. Park, "New CMOS linear transconductor," Electronics Lett., vol. 28, no. 21, pp. 1962–1964, Oct. 8, 1992. | [5] Le-Thai Ha, N. Huy-Hieu, N. Hoai-Nam, C. Hong-So, L. Jeon-Seon, and L. Sang-Gug, "A new low-distortion transconductor applied in a flat bandpass filter," in Proc. | IEEE Asian Solid-State Circuits Conf. (ASSCC'09), Taipei, Taiwan, 2009, pp. 37–40. | [6] S. Lerstaveesin, M. Gupta, D. Kang, and S. B. Sup, "A 48–860 MHz CMOS low-if direct-conversion DTV tuner," IEEE J. Solid-State Circuits, vol. 43, no. 9, pp. 2013–2024, Sep. 2008. | [7] W. B. Kuhn, N. K. Yanduru, and A. S. Wyszynski, "Q-enhanced LC bandpass filters for integrated wireless applications," IEEE Trans. Microw. Theory Tech., vol. 46, no. 12, pt. 2, pp. 2577–2586, Dec. 1998. | [8] A. N. Mohieldin, E. Sanchez-Sinencio, and J. Silva-Martinez, "A 2.7-V 1.8-GHz fourth-order tunable LC bandpass filter based on emulation of magnetically coupled resonators," IEEE J. Solid-State Circuits, vol. 38, no. 7, pp. 1172–1181, Jul. 2003. | [9] B. Georgescu, H. Pekau, J. Haslett, and J. McRory, "Q-enhanced LC bandpass filters for integrated wireless applications," IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process., vol. 50, no. 10, pp. 705–713, Oct. 2003. | [10] D. Hernandez-Garduno and J. Silva-Martinez, "Continuous-time common-mode feedback for high-speed switched-capacitor networks," IEEE J. Solid-State Circuits, vol. 40, no. 8, pp. 1610–1617, Aug. 2005. | [11] M. Trakimas and S. Sonkusale, "A 0.5 V bulk-input operational transconductance amplifier with improved common-mode feedback," in Proc. IEEE Int. Symp. Circuits and Systems (ISCAS 2007), May 27–30, 2007, pp. 2224–2227.