



Design of Transconductor cell for g_m -c Filter

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ABSTRACT

This paper presents design of operational transconductance Amplifier. This design is developed and simulated in 0.35µm CMOS Tanner Environment. This OTA having a biasing current of 2.2 µA with supply voltage ±1.8 V. Simulated Result of this OTA shows the open loop gain of about 60 dB, CMRR 78dB and PSRR of 82dB. This OTA having power dissipation of 7.6 mW and Slew Rate 2.0 V/µsec.

Keywords: Operational Transconductance Amplifier, Gm Cell, Analog Filter

I. INTRODUCTION

The OTA (Operational Transconductance Amplifier) is widely used in analogue circuit such as neural networks, Instrumentation amplifier, ADC and Filter circuit. The operational Transconductance Amplifier (OTA) is basically similar to conventional Operational Amplifiers in which both having Differential inputs. The basic difference between OTA and conventional operational Amplifier is that in OTA the output is in form of current but in conventional Op-Amps output is in form of Voltage[1]. OTA is widely used in the High frequency operation due to tuning ability and linearity[2]. This Design is applicable to the Gm-C (Transconductance –Capacitor) filter.

This paper is organized as follows. Section II describes brief description about operational Transconductance Amplifier (OTA) design. Section III describes Simulation Results of OTA. Section IV describes the conclusion of this paper.

II. OTA DESIGN SCHEMATIC

Figure1.1 shows the schematic diagram of OTA. In this OTA the supply voltage is VDD= +1.8V and VSS= -1.8V. In the below circuit of OTA the Nbias voltage limits the current flow through NM3. The Transistors NM0 and NM1 are the Differential inputs. PM2 and PM3 are to use for gain enhancement stages. DC biasing is done by using the Nbias and Pbias voltage which is directly depends upon the gain of the circuit. The Transistor NM5 is an output amplifier stage. The design parameters of this OTA are shown in below table 1.

PM0 and PM are identical PMOS having a same size to deliver the equal dc current 1.1 µA. PM4 act as a active resistance. NM1 and NM2 delivering the currents as follows:-

$$i_{DNM1} = i_{DNM1} + i_{DNM1} \tag{1}$$

And similarly

$$i_{DNM2} = i_{DNM2} + i_{DNM2} \tag{2}$$

Corresponding output voltage drives the PM3, which is the delivering the current at the output terminal.

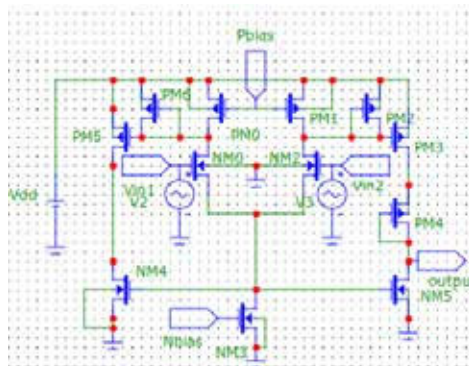


Figure 1: Operational Transconductance Amplifier

MOS	Sizes	MOS	Sizes
NM0	5µm/.35µm	PM1	2µm/.35µm
NM2	5µm/.35µm	PM2	2µm/.80µm
NM3	4µm/.60µm	PM3	2µm/..35µm
NM4	4µm/.60µm	PM4	3µm/.35µm
NM5	5µm/.60µm	PM5	3µm/.35µm
PM0	2µm/.35µm	PM6	2µm/.80µm

Table1: Transistor Sizing

III. SIMULATION RESULTS

The design of this Operational Transconductance Amplifier (OTA) is done using Cadence Tool. The Simulation results are done using Tanner environment using 0.35 µm CMOS technology. The simulation result of the OTA shows that the open loop gains of approximately 65 dB. The OTA has GBW of about 35 KHz.

The Table II shows that the simulated results of the OTA. The AC response which shows gain and phase change with frequency is shown in figure 2. Figure 3 shows the DC sweep response of This OTA. The Transient response with input in pulse is shown in figure 4. Figure 5 illustrates PSRR variations with frequency. The variation in CMRR is shown in figure 6. Values of Nbias and Pbias are 0.6 V and 1.3 voltages respectively.

The simulated results of this OTA shows that PSRR of 85 dB and CMRR of 90 dB.

Specifications	Simulated Values
CMOS technology	0.35µm
Open loop gain	65 dB
Supply voltage	±1.8 V
Load capacitance	6pF
PSRR	85 dB
CMRR	90 dB

Simulation Results

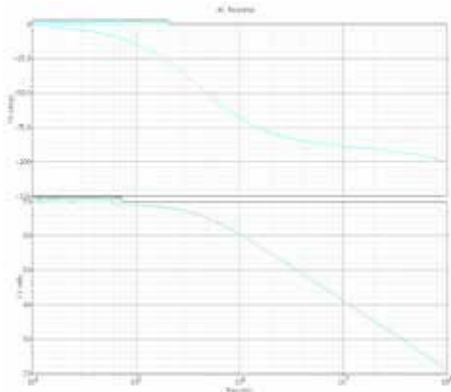


Figure 2: Shows AC response which shows gain and phase change with frequency.

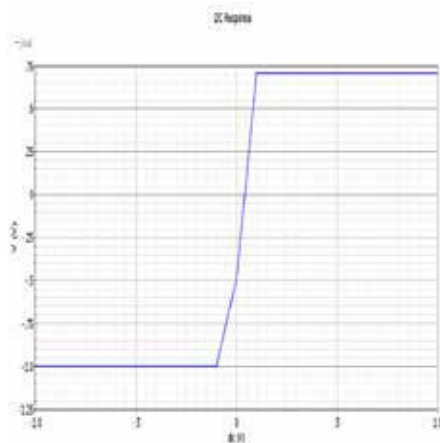


Figure 3: DC sweep response

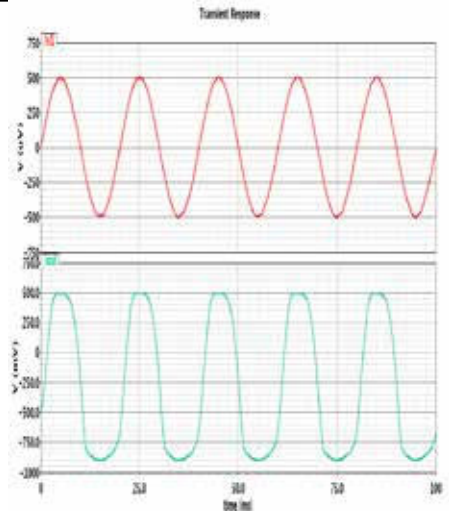


Figure 4: Transient response with input is pulse

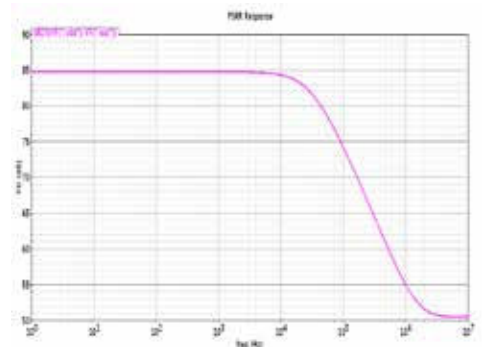


Figure 5: PSRR change with frequency

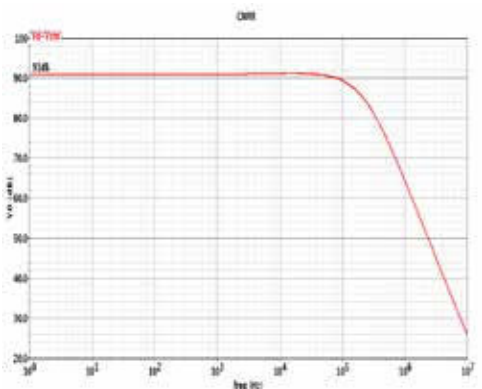


Figure 6: Change in CMRR with frequency

IV. CONCLUSION

In this paper we present a simple Operational Transconductance Amplifier (OTA) topology for low voltage and low power applications. This OTA can be used in low power, low voltage and high time constant applications such process controller, physical transducers and small battery operated devices. This work can be used in filter design, ADC design and instrumentation amplifiers because of its high gain, high CMRR and low power consumption.

REFERENCES

[1]. Phillip E. Allen and Douglas R. Holberg "CMOS analog circuit design", second edition, Oxford university press, 2007,pp. 269-274. | [2]. J. H. Botma, R.F. Wassenaar, R. J. Wiegerink, "A low voltage CMOS Op Amp with a rail-to-rail constant-gm input stage and a class AB rail-to-rail output stage", IEEE 1993 ISCAS, Chicago, pp.1314-1317. | [3]. Paul R. Gray, Paul L.Hurst, Stephan H.Lewis and Robert G.Mayer "Analysis and design of analog integrated circuits",Forth Edition, John Wiley & sons, inc.2001, pp.425-439. | [4]. Adel S. Sedra, Kenneth C.Smith "Microelectronic Circuits", Oxford university press, Fourth edition ,2002,pp.89-91. | [5]. Jin Tao Li, Sio Hang Pun, Peng Un Mak and Mang I Vai "Analysis of Op-Amp Power-Supply Current Sensing Current-Mode Instrumentation Amplifier for Biosignal Acquisition System",IEEE conference,August-2008,pp.2295-2298. | [6]. Y. Tsvividis, Operation and Modeling of the MOS Transistor, 2nd ed. Boston, MA: McGraw-Hill, 1998. | [7]. D. A. Johns and K. Martin, Analog Integrated Circuit Design. New York: Wiley, 1997. |