



Design of two Stage High Gain Opamp

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ABSTRACT

A High Swing Ultra-Low-Power Two Stage CMOS OP-AMP in 0.18 μm Technology with 1.2v supply, is presented. Cascode technique has been used to increase the dc gain. The unity-gain bandwidth is also enhanced using a gain-stage in the Miller capacitor feedback path. The proposed opamp provides 236MHz unity-gain bandwidth, 109.7 degree phase margin. The circuit has 94.34dB gain. The power dissipation of the designed only is approximately 50 μw . The designed system demonstrates relatively suitable response in different temperature.

Keywords:

(1) Introduction:-

Operational Amplifiers (Op amps) are one of the most widely used building blocks for analog and mixed-signal systems. They are employed from dc bias applications to high speed amplifiers and filters. General purpose op amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications. With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modeling, steady miniaturization of transistor scaling, and the progress of fabrication processes, the integrated circuit market is growing rapidly. Nowadays, complementary metal-oxide semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design in a mixed-signal system due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip. While many digital circuits can be adapted to a smaller device level with a smaller power supply, most existing analog circuitry requires considerable change or even a redesign to accomplish the same feat. With transistor length being scaled down to a few tens of nanometers, analog circuits are becoming increasingly more difficult to improve upon.

The operational amplifier is one of the most useful and important components of analog electronics. They are widely used in popular electronics. Their primary limitation is that they are not especially fast: The typical performance degrades rapidly for frequencies greater than about 1 MHz, although some models are designed specifically to handle higher frequencies.

The primary use of op-amps in amplifier and related circuits is closely connected to the Concept of negative feedback. Feedback represents a vast and interesting topic in itself. We will discuss it in rudimentary terms a bit later. However, it is possible to get a feeling for the two primary types of amplifier circuits, inverting and non-inverting, by simply postulating a few simple rules (the 'golden rules'). We will start in this way, and then go back to understand their origin in terms of feedback.

(2) Basic Block diagram CMOS op-amp:-

Operational Amplifiers are the backbone for many analog circuit designs. Op-Amps are one of the basic and important cir-

cuits which have a wide application in several analog circuits such as switched capacitor filters, algorithmic, pipelined and sigma delta A/D converter, sample and hold amplifier etc. The speed and accuracy of these circuits depends on the bandwidth and DC gain of the Op-amp. Larger the bandwidth and gain, higher the speed and accuracy of the amplifier Op-amp are a critical element in analog sampled data circuit, such as SC filters, modulators. The general block diagram of an op-amp with an output buffer is shown below

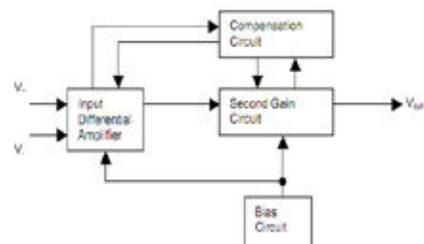


Figure 1. Block diagram of Op-Amp

The first block is a differential amplifier. It has two inputs which are the inverting and non-inverting voltage. It provides at the output a differential voltage or a differential current that, essentially, depends on the differential input only. The next block is a differential to single-ended converter. It is used to transform the differential signal generated by the first block into a single ended version. Some architecture doesn't require the differential to single ended function; therefore the block can be excluded. In most cases the gain provided by the input stages is not sufficient and additional amplification is required. This is provided by intermediate stage, which is another differential amplifier, driven by the output of the first stage. As this stage uses differential input unbalanced output differential amplifier, so it provide required extra gain. The bias circuit is provided to establish the proper operating point for each transistor in its saturation region. Finally, we have the output buffer stage. It provides the low output impedance and larger output current needed to drive the load of op-amp or improves the slew rate of the op -amp. Even the output stage can be dropped: many integrated applications do not need low output impedance; moreover, the slew rate permitted by the gain stage can be sufficient for the application. If the op-amp is intended to drive a small purely capacitive load, which

is the case in many switched capacitor or data conversion applications, the output buffer is not used. When the output stage is not used the circuit, it is an operational transconductance amplifier, OTA. The purpose of the compensation circuit is lower the gain at high frequencies and to maintain stability when negative feedback is applied to the op amp.

A. Circuit Operation The final circuit designed to meet the required specifications is shown in Figure 2. The topology of this circuit is that of a standard CMOS op-amp. It comprised of three subsections of

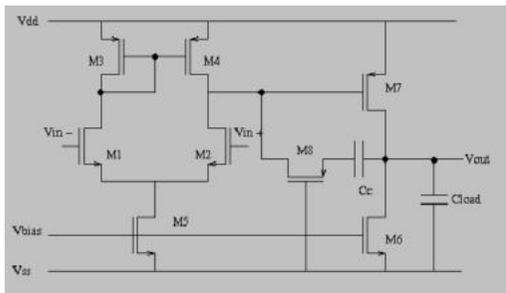


Figure2. The topology chosen for this Op-Amp design.

Circuit, namely differential gain stage, second gain stage and bias strings. It was found that this topology was able to successfully meet all of the design specifications.

B. Differential Gain Stage

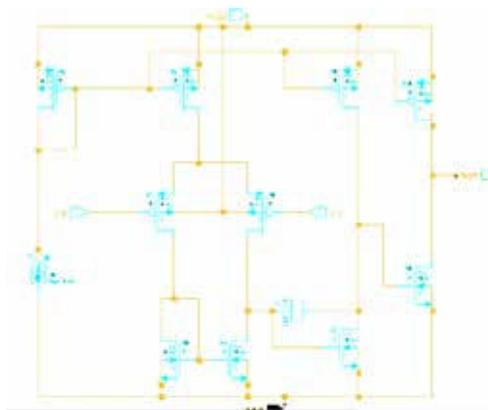
Transistors M1, M2, M3, and M4 form the first stage of the op amp the differential amplifier with differential to single ended transformation. Transistors M1 and M2 are standard N channel MOSFET (NMOS) transistors which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The gain of the stage is simply the transconductance of M2 times the total output resistance seen at the drain of M2. The two main resistances that contribute to the output resistance are that of the input transistors themselves and also the output resistance of the active load transistors, M3 and M4. The current mirror active load used in this circuit has three distinct advantages. First, the use of active load devices creates a large output resistance in a relatively small amount of die area. The current mirror topology performs the differential to single-ended conversion of the input signal, and finally, the load also helps with common mode rejection ratio. In this stage, the conversion from differential to single ended is achieved by using a current mirror (M3 and M4). The current from M1 is mirrored by M3 and M4 and subtracted from the current from M2. The differential current from M1 and M2 multiplied by the output resistance of the first stage gives the single-ended output voltage, which constitutes the input of the second gain stage.

C. Second Gain Stage The second stage is a current sink load inverter. The purpose of the second gain stage, as the name implies, is to provide additional gain in the amplifier. Consisting of transistors M5 and M6, this stage takes the output from the drain of M2 and amplifies it through M5 which is in the standard common source configuration. Again, similar to the differential gain stage, this stage employs an active device, M6, to serve as the load resistance for M5. The gain of this stage is the transconductance of M5 times the effective load resistance comprised of the output resistances of M5 and M6. M6 is the driver while M7 acts as the load.

(3)Design of the op-amp

The design in this project is a two-stage op amp with an n-channel input pair. The op amp uses a dual-polarity power supply (Vdd and Vss) so the ac signals can swing above and

below ground and also be centered at ground. The hand calculation results provided the estimated parameters (such as transistor width and length, capacitance, etc.) to make the circuit schematic (shown in figure) in Design Architect IC and for the circuit analysis in Model Sim Eldo of Mentor Graphic Tool. Schematic used in this design is



Design of two stage opamp using mentor graphics

(4)Simulation Result

Using Mentor Graphics EDA Tool we have design High Swing Ultra-Low-Power Two Stage CMOS OP-AMP as shown in schematic window. Fig 1 & Fig 2 shows the Gain and Phase plot for basic two stage opamp. After simulation we have analyzed that the gain of the opamp is 94.34db and have a phase margin of 109.7 degree at 40 MHz frequency. This analysis can be made possible using different sizing of the MOS transistor at different stages. There graphs are as

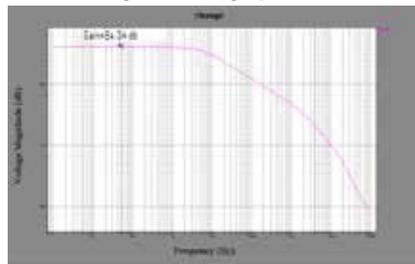


Fig. 1 Gain graph

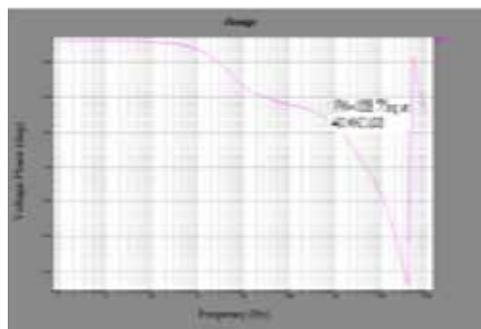


Fig.2 phase margin plot

From the reference paper[14] we have seen that the gain is 90 db which is improves up to 94.3db which is used in any of Analog designing.

Table shows the brief of results as

GAIN	94.34 db
PHASE MARGIN	104.7° at 40MHZ

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