Research Paper Engineering

Level Converter for Multi-V_{DD} Systems with High Performance Multi Threshold Voltage

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ABSTRACT

Multiple voltage supply systems are most efficient and commonly employed techniques for low power designs. The idea behind this technique is to use multiple supply voltages (multi-VDD) for a single chip by dividing the integrated circuit into regions, called voltage islands, operating at different voltages. In dual supply voltage circuits, when connecting a circuit having low voltage supply(VDDL) to a circuit having high voltage supply (VDDH), it is necessary to insert level converter at each low-to-high boundary as the interface to prevent the flow of static current. In this paper we have characterized the previously proposed Multi-Threshold voltage based level converters as well as proposed a new high performance level converter using Cadence Virtuoso tool in UMC 180nm standard CMOS technology. The proposed design offers up to 38.10% power reduction and up to 50.88% less Power Delay Product (PDP) than the existing level converters.

Keywords: Multi threshold voltage, Level Converter, Multi-VDD System, Power Delay Product (PDP).

I. INTRODUCTION

As the use of the portable electronic devices increases very rapidly, low-power becomes a very important circuit design issue. Research and development in this field are motivated by growing markets of portable information devices, such as PDA's, cellular phones, digital cam-coders and digital cameras. For VLSI's in those applications, high performance and low power are required simultaneously. High performance is required for data processing such as real-time encoding and decoding of picture/audio data, while low power for prolonging battery life. Requirement for power minimization is not limited to portable applications. In consumer applications in which cost competition is extremely serious, low power is needed for reducing package cost. Power must be low if one uses cheap plastic packages instead of expensive ceramic ones. Power minimization is also required for improving reliability of high-end microprocessors. Operation frequencies are raised for improving performance in those VLSI's, resulting in increasing power (current) dissipation. This tends to cause reliability problems such as electro-migration in wires, hot electron effects in MOS transistors, IR- drop in power lines and ground bounce. Power reduction technologies keeping high performance are strongly required.

In CMOS VLSI circuits, lowering the power-supply voltage (V_D) is an effective way of the low-power design, because it results in a quadratic reduction in dynamic power consumption and an exponential reduction in leakage power consumption [2]. However, lowering the V_{DD} of the whole system degrades the operating speed.

To reduce power consumption while avoiding the speed degradation, there is an approach which uses dual supply voltages one high, $V_{DDH,}$ and the other low, . So that the circuit part on the critical path is operated with V_{DDH} and the circuit part off the critical path is operated with V_{DDL}. This results in reducing the power without degrading the entire circuit performance. Advantages of this approach are: 1) no need of changing V_{th} and hence no need for changing the regular fabrication process; 2) no need for creating parallel/pipelined data-paths causing heavy area penalty or undesired increase in latency.

However, this approach has a problem when implementing in CMOS circuits. Static current flows at a V_{DDH} gate if it is directly driven by a V_{DDL} gate. This is because the PMOS at the V_{DDH} gate cannot be cut-off at the input level "High". A typical way of blocking the static current is to insert a level converter circuit into the interface of a V_{DDL} gate to a V_{DDH} gate.

The level converter is a key circuit component in multi-voltage circuits and has important implementation. Since the level converter circuit consumes power and has a considerable delay, how to optimize the performance to gain low power and small delay and how to minimize the number of level converters are important in the voltage scaling technique. In this paper, we have optimized two level converters previously reported [2] based on multi-threshold voltage CMOS technology and proposed a new level converter. The new level converter is compared with the two previously published level converters for different supply voltages.

The paper is organized as follows. A brief description of the previously reported level converter is given in Section II. Section III presents the details of proposed level converter. The power consumption and the propagation delay comparison of the level converters are presented in Section IV. Finally, some conclusions are provided in Section V.

II. PREVIOUSLY REPORTED LEVEL CONVERTERS

In this section, first we present a brief description of the need of level converter. As shown in Fig. 1 If a gate is directly connected to a V_{DDH} gate, the voltage at the Node N2 is not raised higher than even at the logic "HIGH" level. The PMOS device at the V_{DDH} gate, which should be off under this condition, will be rather weakly ON, resulting in the flow of static current from the supply to ground. This becomes a serious problem in low-power CMOS circuits. A typical way of blocking the static current is to insert a level-converter circuit between a low voltage driver and a full voltage swing receiver. The level

converter converts the voltage swing from V_{DDL} to V_{DDH}.

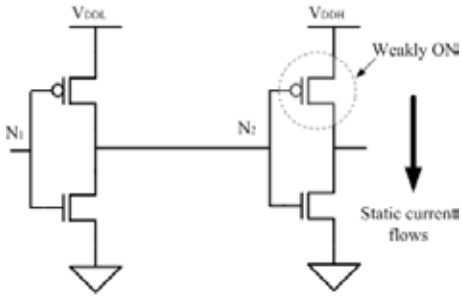

Fig.1. Direct connection of VDDL gate to VDDH gate

Fig. 2(a) and Fig 2(b) show two level converters that have been reported previously [2]. Fig. 2(a) shows a first Multi-V_{th} level converter (MLC1). The Multi-V_{th} level converters utilize a Multi-Threshold CMOS (MTCMOS) technology in order to eliminate the static dc current. The high threshold voltage pull-up transistors in this level converter are directly driven by the low level signals without producing a static dc current problem. The first level converter is composed of two cascaded inverters with dual-Vth transistors. The threshold voltage of M2 (V_{th}-*M2*) is high (higher $|V_{th}|$). The threshold voltage $|$Vth-M2$|$ is required to be higher than V_{DDH}-V_{DDL} for eliminating the static dc current in the first inverter when the input is at V_{DDL}. The Multi-Vth level converter operates as follows: When the input is at 0 V, M2 is turned on and M1 is cutoff. Node A is pulled up to V_{DDH}.

The output is discharged to 0 V. When input rises to V_{DDL}, M1 is turned on and M2 is turned off since VGS, M2 > Vth, M2. Node A is discharged to 0 V and the output is charged to V_{DDH}.

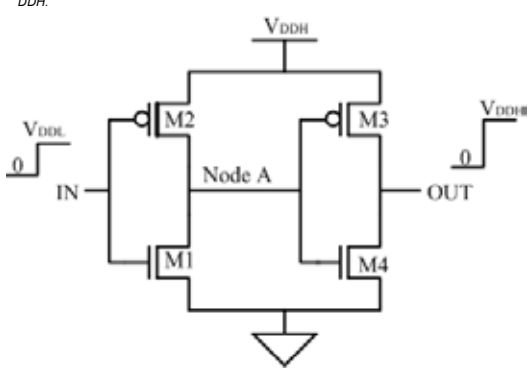

Fig. 2. (a) First multi-Vth level converter (MLC1) presented in [2]. Thick line in the channel area indicates a high-Vth device

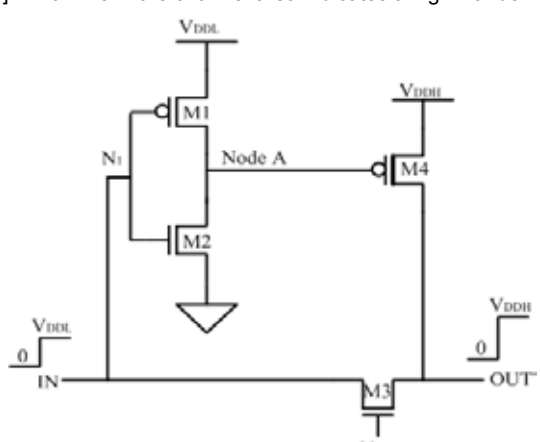

Fig.2. (b) Second level converter (MLC2) presented in [2]. Thick line in the channel area indicates a high-Vth device

The circuit configurations of the second Multi-Vth level Converter (MLC2) is shown in Fig. 2(b) for enhancing the speed as compared to MLC1. $|V_{th\text{-}M4}|$ is required to be higher than $V_{DDH} - V_{DDL}$ for eliminating the static dc current when the input is low (Node A is at V_{DDL}). In this level converter when the input is at 0 V, Node A is pulled high (V_{DDL}) turning M4 off .The output node is discharged to 0 V through the pass transistor M3. When the input rises to V_{DDL}, the output node is initially charged to and V_{DDL}-$V_{th\text{-}M3}$ through M3. M4 is turned on after the high-to-low transition of the node A. The output is pulled high all the way up to V_{DDH} through M4. M3 is turned off isolating the two power supplies. Both M3 and M4 assist the output low-to-high transition. The speed of MLC2 is enhanced due to the shorter input-to-output signal propagation path.

III. PROPOSED LEVEL CONVERTER DESIGN

As we have seen, to avoid excessive power consumption between the low and high voltage regions, level converters should be inserted. In this section, we propose a new high performance multi threshold level converter for low-to-high supply voltage transition.

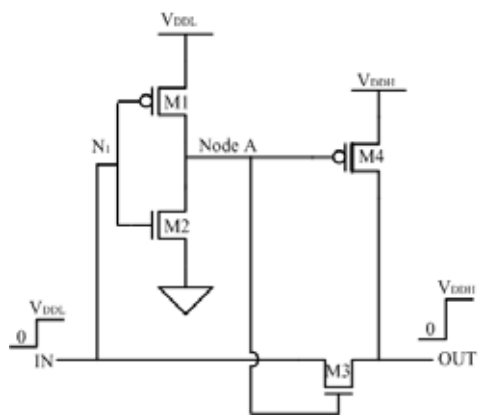

Fig. 3 (PMLC) The proposed new level converter.

The circuit configuration of the proposed level converter (PC) for operation at different supply voltages is shown in Fig. 3. In this configuration $|V_{th\text{-}M4}|$ is required to be higher than V_{DDH}-V_{DDL} for eliminating the static dc current when the input is low (Node A is at V_{DDL}). In the proposed level converter the pass transistor M3 is driven by the input stage inverter rather than by direct supply voltage as in the existing multi threshold level converter MLC2 (shown in Fig. 2(b)) due to this the contention at output node decreases and hence the power dissipation in this level converter decreases. PC operates as follows, when the input is at 0 V, Node A is pulled high to V_{DDL} turning M4 off and M3 on. The output node is discharged to 0 V through the pass transistor M3. When the input transitions to V_{DDL}, node A is pulled down to 0 V turning M4 on and M3 off. When M4 is turned on after the high-to-low transition of node A, the output is pulled high all the way up to V_{DDH} through M4. M3 is turned off isolating the two power supplies. In proposed level converter only M4 assist the output from low-to-high transition. Hence eliminates the contention current and reducing the total energy consumption.

IV. SIMULATION AND COMPARISON

All the circuits were implemented in Cadence Virtuoso tool using the professional foundry UMC 180nm standard CMOS technology for the following values of VDDL: 0.7, 1, and 1.2V. The high supply voltage (VDDH) used for implementation is 1.8V. The simulation results of these level converters are given in Table 1 which compares their performance in terms of their power consumption, delay and power delay product (PDP) and the comparison is plotted graphically in Figs. 4, 5 and 6.

TABLE I
COMPARISON OF LEVEL CONVERTERS, POWER AND PERFORMANCE AT THE MINIMUM PDP POINT

V_{DDL}	Level Converter	Power (µw)	Delay (ps)	PDP (fJ)
1.2 V	MLC1	1.226	135.68	0.166
	MLC2	1.145	97.66	0.1118
	PMLC	0.9056	105.84	0.0958
1 V	MLC1	1.6146	145.95	0.2356
	MLC2	1.497	125.05	0.187
	PMLC	1.047	134.6	0.1409
0.7 V	MLC1	3.668	396.15	1.453
	MLC2	3.386	290.95	0.985
	PMLC	2.2702	314.35	0.7136

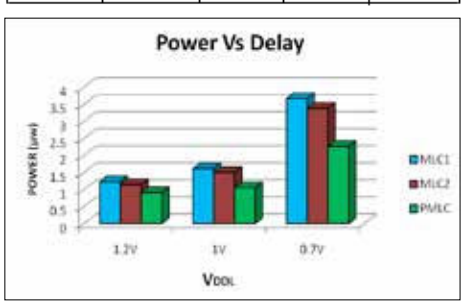

Fig. 4 Plot for power vs input voltage for different level converters.

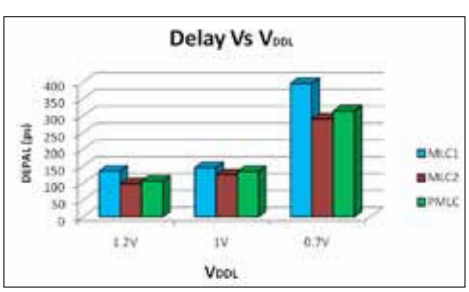

Fig. 5: Plot for Delay vs input voltage for different level converters.

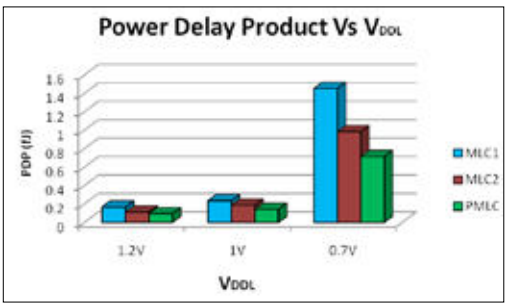

Fig. 6: Plot for Power Delay Product vs input voltage for different level converters.

V. CONCLUSION

In this paper, we have proposed a new level converter for a multi-VDD system. The proposed level converter provides the level up conversions for the various input voltage levels. The proposed level converter is compared with the previously published level converters. Simulation show that the proposed level converter offers significant power saving of up to 38.10% as compared to the previously published level converters. The proposed level converter is up to a 21.99% faster than the existing level converter [MLC1], but it is slightly slower than the existing level converter [MLC2]. The speed of the proposed level converter decreases up to 8.04% than MLC2. Despite the above, the proposed level converter shows an overall improved performance by exhibiting up to 14.31 ~ 50.88% less PDP than the existing level converters.

VI. ACKNOWLEDGMENT

The authors gratefully acknowledge for utilizing the facilities of VLSI Lab under S. M. D. P. II program sponsored by Ministry of Communication and Information Technology, Govt. of India, in the Dept. of Electronics Engineering IIT (BHU) Varanasi.

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