Research Paper Engineering

Simulation and Performance Evaluation of Total Harmonic Distortion And Fft Analysis in Multi Carrier Nine-Level Cascade H- Bridge Inverter Using Psim

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ABSTRACT

This paper presents a harmonic analysis in terms of Total Harmonic Distortion (THD) and Fast Fourier transformation (FFT) for a Nine level cascaded H-Bridge Multi level inverter(CHB-MLI) with phase shift PWM and level shifted PWM. The performance indices of the proposed system are simulated using PSIM and tabulated. Various level shift PWM techniques like Phase Displacement (PD), Phase opposition Displacement (POD), Anti Phase opposition Displacement (APO), variable frequency (VF) and Carrier overlap (CO) is discussed. It is inferred from the simulation that THD and FFT of COPWM is low.

Keywords : Multi Carrier PWM, Level Shifted PWM, Multilevel inverter, phase shifted PWM, PSIM, NPC, FC, EMI, SDCC and CHB

I. Introduction

In the last decade, medium-voltage high-power converters have become widely used as drives for pumps, fans and material transport in a number of industries, as well as for VAR compensation in grid applications [1], [2]. At this voltage range, multilevel inverters are preferred to overcome the voltage blocking limitations of the available switches. Another important advantage of this technology is the improved output waveforms due, to the higher number of levels in the output voltage waveform, compared to the conventional three-phase two-level inverter. Similarly, an increased number of voltage levels will result in a reduced input filter size for grid connected applications. Moreover, a high number of levels allow the device switching frequency to be reduced for a given current distortion.

The multilevel topologies can be classified into three main categories: the neutral point clamped (NPC) [3], the flying capacitors (FC) [4], [5] and the cascaded H-bridge (CHB) converters [6], [7]. The three level NPC Bridge is probably the most widely used topology for medium voltage AC motor drives and PWM active rectifiers [8], [9]. NPC converters with more levels are also possible, although there are significant problems in the balancing of their dc-link capacitor voltages [10], [11], unless modified modulation strategies [12] or additionally circuitry [13] are used. On the other hand, the CHB converter is normally implemented with large number of levels, but at the cost of complicated and bulky input transformers with multiple rectifiers [7], [14], [15] or multi-winding three-phase output transformers .

For the NPC inverter, various carrier based PWM schemes have been investigated and proposed by Carrara [3].This paper proposes various switching methodology of phase shift PWM and Level shift PWM using PSIM software. The paper is arranged such that section 2 introduces the operation of CHB, section 3 explains about various PWM control techniques for multilevel inverter, section 4 presents the simulation of proposed system, section 5 discuss about the results and section 6 with conclusion.

II Cascaded H-bridge Topology (CHB)

A. Construction and operation

It is the series connection of the single phase H-bridge units with separate DC sources (SDCSs). These SDCSs may be batteries,

fuel cells or solar cells [4].

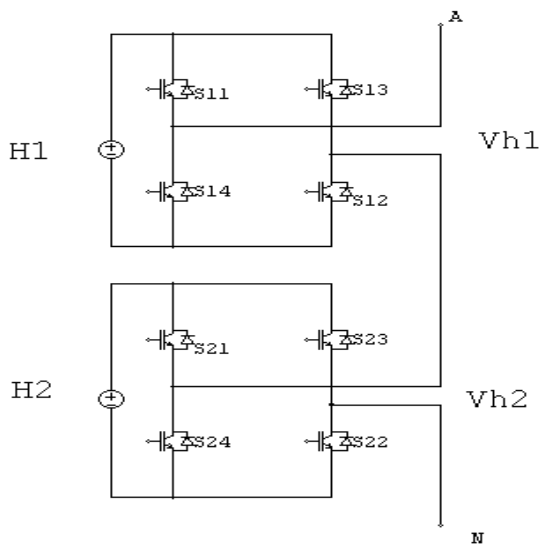

Fig. 2.1. Basic circuit diagram of CHB

Each unit produces three voltages at the output: + V_{dc}, 0, and – V_{dc}. The number of these units is decided by the operating voltage and manufacturing cost [5]. This topology of inverter is suitable for high voltage and high power inversion because of its better harmonic spectrum with low switching frequency.

Fig. 2.1 shows a phase leg of a five level cascaded inverter. It consists of two H-Bridge inverter units with two isolated and equal DC sources. When switches S_{11}, S_{21} and switches S_{12}, S_{22} conduct, the output voltage of the H Bridge is $VH_1 = VH_2 = +E$ and the resultant inverter phase voltage is $V_{AN} = VH_1 + VH_2 = 2E$.

This switching state redundancy provides a greater flexibility for switching pattern design. The number of the output line voltage level is found by m= (2H+1) where H is the number of H-bridges in each phase leg. Unlike other multilevel inverters, only odd number of voltage level is obtained in CHB. The total number of active switches used in CHB is given by

N_{sw}=6(m-1). (1)

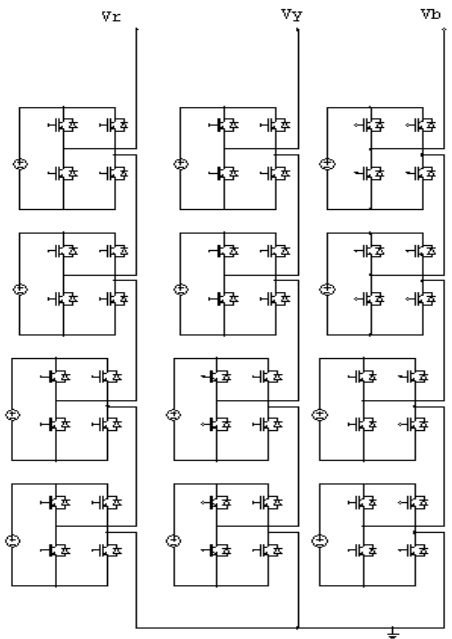

Fig 2.2 Nine level cascaded multi level inverter

Fig.2.2 shows an IGBT based three phase nine level cascaded inverter.

III.Multi level inverter modulation control schemes

A.VARIOUS TYPES OF MODULATION

Figure 3.1 shows the multilevel converter modulation methods. The modulation control schemes for the multilevel inverter can be divided into two categories, fundamental switching frequency and high switching frequency PWM such as multilevel carrier-based PWM, selective harmonic elimination and multilevel space vector PWM Multilevel SPWM needs multiple carriers. Each DC source needs its own carrier. By generalizing, for an 'n' level multilevel inverter, (n-1) carriers are needed. The implementation of the various carrier PWM techniques that is possible for multi-level inverters are [3]-[6]:

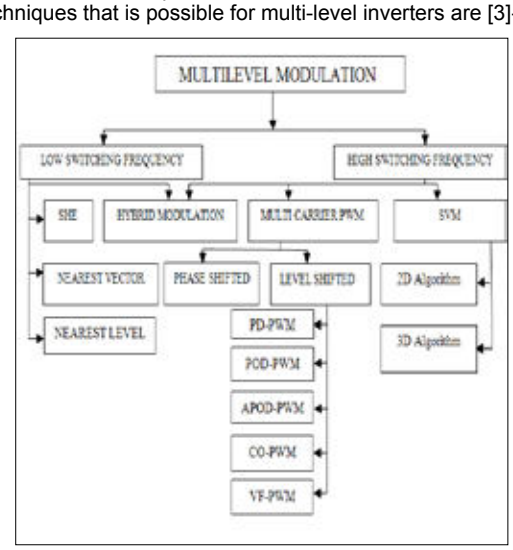

Fig 3.1 Classification of modulation strategy of MLI

B.PHASE OPPOSITION DISPOSITION (POD) PWM

This technique requires four carrier waveforms that are all in phase above or below the zero reference value. However, they are phase shifted by180° between the carrier waveforms above and below zero.

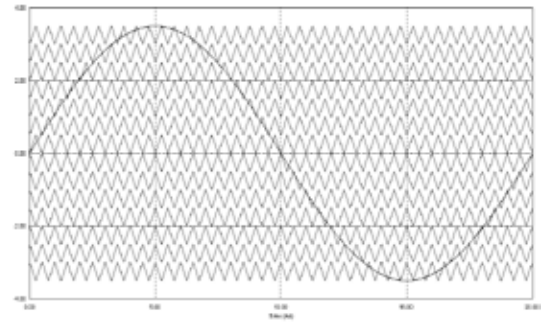

Fig3.2: Generation of PWM using POD

C.PHASE DISPOSITION (PD) PWM

With the wide application in multi-level inverters, this technique has all carriers in phase. It requires four carrier waveforms. The zero reference is placed in the middle of the carrier sets.

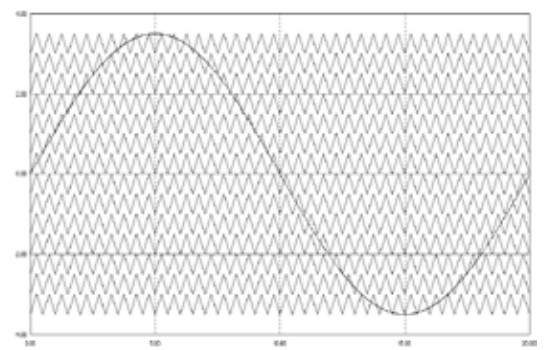

Fig3.3: Generation of PWM using PD

D.ALTERNATIVE PHASE OPPOSITION DISPOSITION (APOD) PWM

This technique requires four carrier waveforms, which are phase-displaced by 180° alternately.

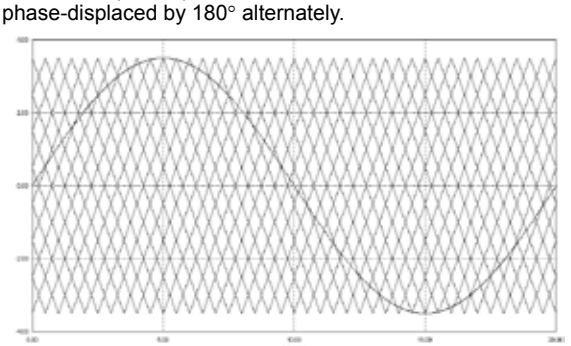

Fig 3.4: Generation of PWM using APOD

E.CARRIER OVERLAB (CO) PWM

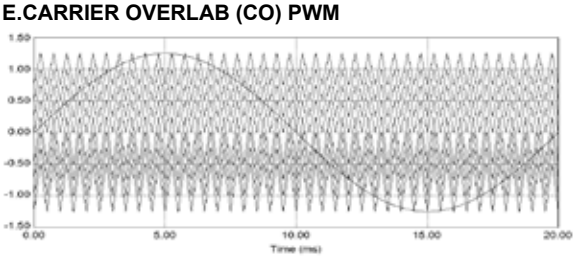

Fig3.5: Generation of PWM using Carrier overlap

For an m level inverter using carrier overlap method,m-1 carriers with the same frequency f_c and same peak to peak amplitude A_c are disposed such that the bands they occupy overlap each other; overlapping vertical distance between each carrier is $A_c/2$.The reference waveform has amplitude of A_m and frequency f_m and it is centered in the middle of the carrier signals.

The reference wave is continuously compared with each of the carrier signals. The modulation index m_a and the frequency ratio mf are defined in the carrier overlap method as follows

$$m_a=A_m/((m/4)*A_c) \quad (2)$$

$$m_f=f_c/f_m \quad (3)$$

F.VARIABLE FREQUENCY (VF) PWM

The frequency modulation index

$$mf = fc/fm \quad (4)$$

The amplitude modulation index

$$ma = 2Am/ (m-1) Ac \quad (5)$$

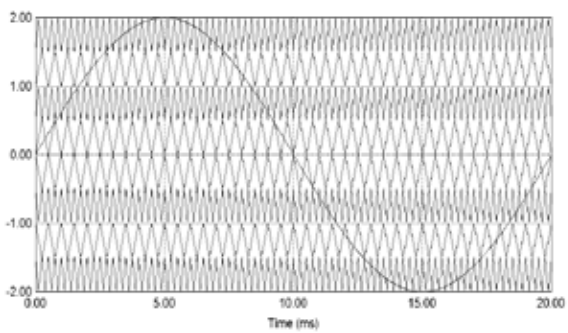

Fig3.6: Generation of PWM using Variable Frequency

where
fc – Frequency of the carrier signal
fm – Frequency of the reference signal
Am –Amplitude of the reference signal
Ac – Amplitude of the carrier signal

$$ma =Am / (m / 4)* Ac \text{ (COPWM)} \quad (6)$$

G. Phase Shifted Multicarrier Modulation

In phase shifted PWM (PS-PWM), there is a phase shift of between the adjacent carrier signals. The phase shift is given by

$$\Phi=360^0/(m-1) \quad (7)$$

For a three phase inverter, the modulating signals should also be three phase sinusoidal signals with adjustable magnitude and frequency. For this modulation scheme, the frequency modulation index f_m and the amplitude modulation index f_a is given by

$$m_f= f_{car}/f_m \quad (8)$$

$$m_a= V_{mod}/V_{car} \quad (9)$$

where f_{car}, f_m are frequency of carrier and modulating signal respectively and V_{car}, V_{mod} are amplitude of carrier and modulating signal respectively.

The switching frequency of the device can be calculated as

$$f_{dev}=f_{car}=f_m \text{ x } m_f \quad (10)$$

The switching frequency of the inverter can be found from the device switching frequency as

$$f_{inverter} = (m-1)f_{dev} \quad (11)$$

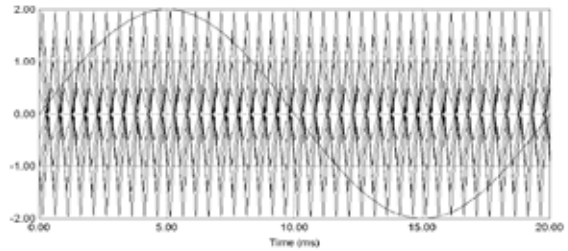

Fig3.7: Generation of PWM using Phase shift

IV.SIMULATION AND RESULTS

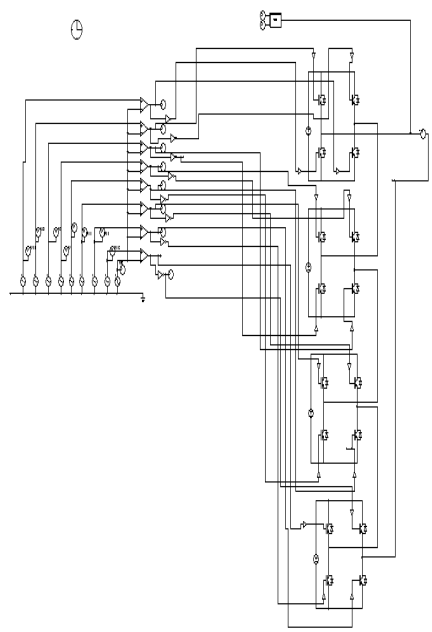

Fig 4.1: Simulation circuit of Nine level inverter using PSIM for single phase

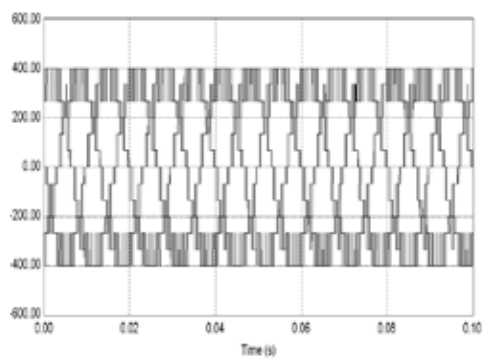

Fig 4.2 :Three phase output voltage using PD-PWM

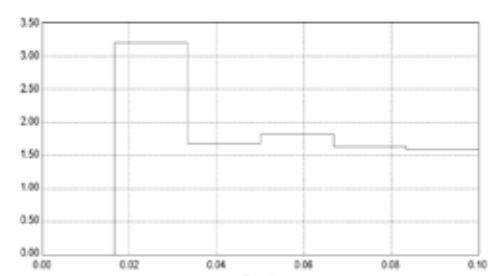

Fig 4.3 : THD of Line voltage using PD-PWM

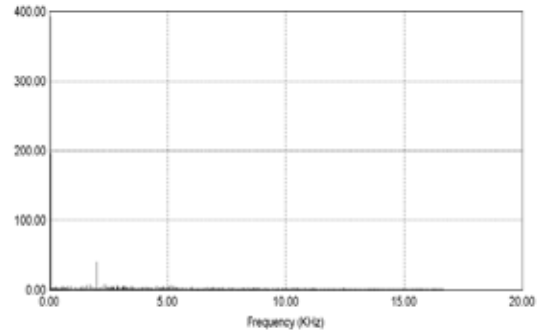

Fig 4.4 : FFT of Line voltage using PD-PWM

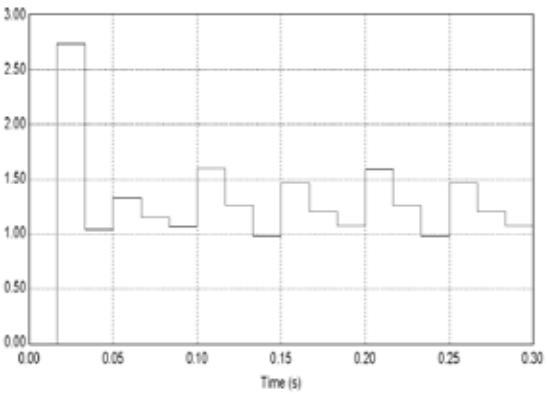

Fig 4.5 : THD of Line voltage using POD-PWM

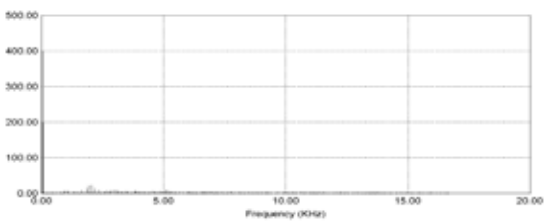

Fig 4.6 : FFT of Line voltage using POD-PWM

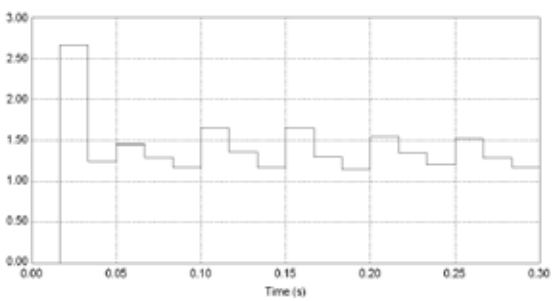

Fig 4.7: THD of Line voltage using APOD-PWM

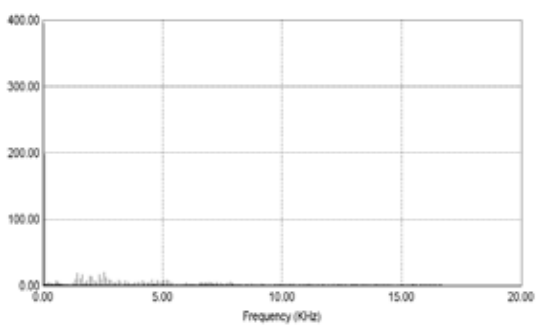

Fig 4.8 : FFT of Line voltage using APOD-PWM

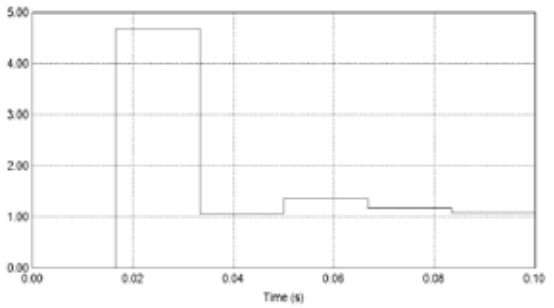

Fig 4.9: THD of Line voltage using PHASE SHIFT-PWM

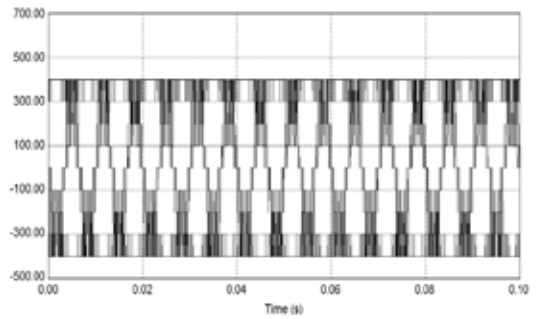

Fig 4.10: Three phase output voltage using Phase shift

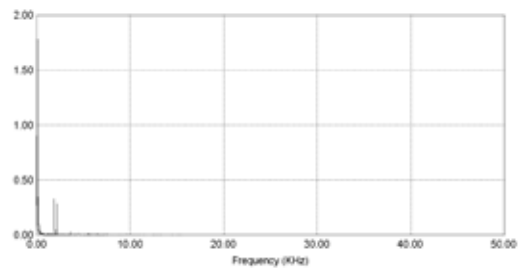

Fig 4.11 : FFT of Line voltage using Phase shift

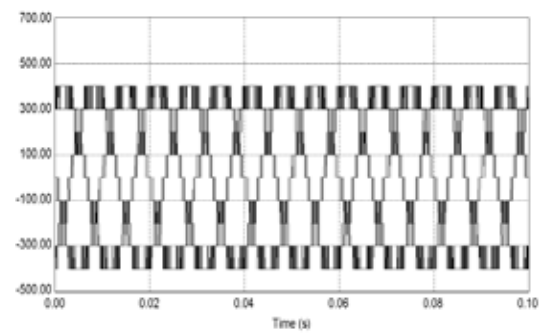

Fig 4.12 : Three phase output voltage using variable frequency

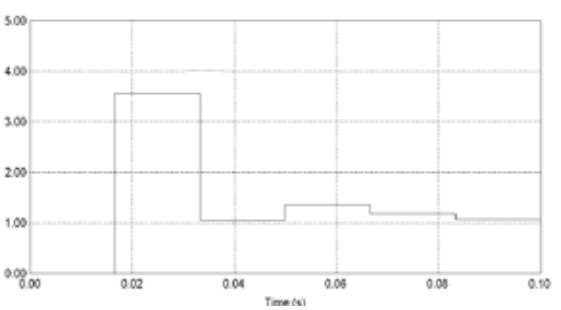

Fig 4.13: THD of Line voltage using VF-PWM

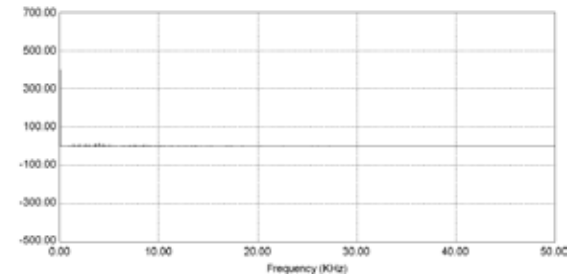

Fig 4.14 : FFT of output voltage using variable frequency

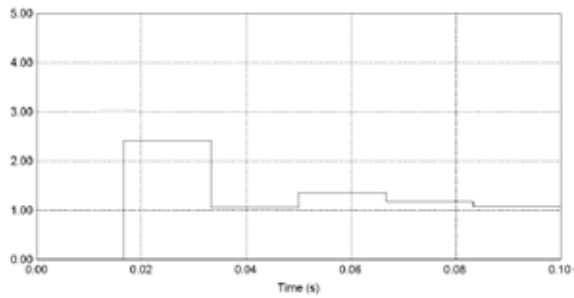

Fig 4.15: THD of Line voltage using CO-PWM

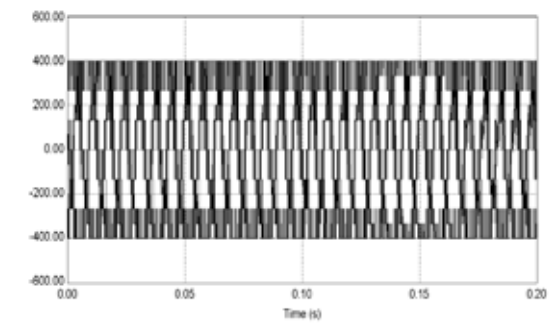

Fig 4.16 : Three phase output voltage using CO-PWM

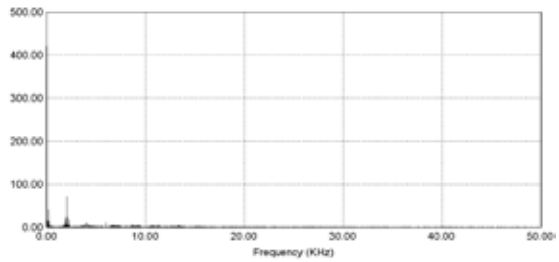

Fig 4.17: FFT of Line voltage using CO-PWM

V TABULATION AND OBSERVATION

THD ANALYSIS TABLE FOR NINE LEVEL INVERTER

LEVEL	LEVEL SHIFT MODULATION					PHASE SHIFT MODULATION
	PD	POD	APOD	CO	VF	
9 LEVEL	3.3	2.75	2.65	2.42	3.5	4.8

Table 1 : Analysis of THD for various PWM methods using simulation for Modulation index (m_a) = 0.7.

V CONCLUSION

Various modulation strategies are compared for a three phase Nine level MLI and their performance indices are tabulated. All methods achieve improvement in line to line voltage harmonics compared to the conventional modulation techniques. From the FFT and THD analysis table of various PWM methods carrier overlap (CO-PWM) shows superior performance than other method. As the output reduces most of the harmonics, the same scheme can be used for grid connected applications.

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