Research Paper Engineering

Analysis Of Quad and Oct System Delay Buffer for Low Power Using Clock Gating Based Gated Driver

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ABSTRACT

As VLSI technology progresses, there is a need for low power consumption in delay buffer during data write in or read out. This paper presents the design of low power in Quad and Oct System delay buffer using clock gating and gated driver tree. It is achieved due to the implementation of double edge triggered (DET) flip flops in ring counter addressing scheme along with the implementation of combinational elements (C-element) in the control logic for generating clock gating signals. Using the clock gated driver tree and gated driver tree both for input and output port of memory reduces the power consumption. The proposed Oct system delay buffer consumes less power than the existing Quad system delay buffer.

Keywords : delay buffer, clock gating, gated driver tree, ring counter.

1. INTRODUCTION

Delay buffers which are also line buffers and delay lines are used in portable battery operated, multimedia and wireless applications like mobile phone, laptop, camera etc. This serial access memory is needed in the temporary storage of signals. To compensate for the difference in the rate of being flow of date, holding data for use at a later timing, allowing timing corrections to be made on data stream, delaying the transit time of signal in order to allow other applications to occur delay buffers are used. Currently, most circuits adopt static random access memory (SRAM) plus some control/addressing logic to implement delay buffers. For smaller-length delay buffers, shift register can be used instead.

In the delay buffer, a gated clock ring counter is used to access the memory. Instead of single edge triggered flip flop, the ring counter uses double edge triggered (DET) flip flop to half the operating clock frequency. In the control logic for generating the clock gating signals to avoid the increasing loading of the global clock signal, combinational element (C-element) is used. In addition to gating the clock signal going to the DET flip flops in the ring counter, a gated clock driver tree is then applied to further reduce the activity along the clock distribution network. If no gating is applied, all drivers need to be activated. A driver tree distribution network is used for the global clock and activate only those drivers along the path from the clock source to the block that need to be activated by the clock. This technique will greatly decrease the loading on distribution network of the clock signal for the ring counter and thus the overall power consumption. The same technique is applied to the input driver and output driver of the memory part in the delay buffer. For the input circuitry, in each level of the driver tree, only one driver along the path leading to the addressed memory word is activated. Similarly, only one driver along the path from the addressed memory word to the output is activated for the read circuitry in each level of driver tree. Thus, the power wasted on the drivers can be eliminated that need not to be activated by this technique.

2. BLOCK DAIGRAM

The system for delay buffer consists of ring counter, gated clock driver, memory, gated input and output driver tree. Grouping of four and eight DET flip flops make Quad system and Oct system.

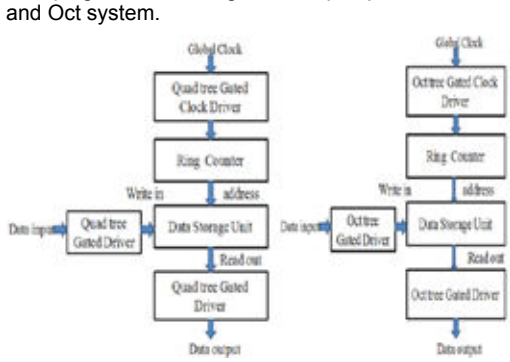

Fig.1: Block diagrams for Quad and Oct system delay buffer.

3. CONVENTIONAL DELAY BUFFERS

For implementing short delay buffers where area and power are of less importance, shift registers are used. Upon the application of clock pulses, data in the shift register can be moved. [2]

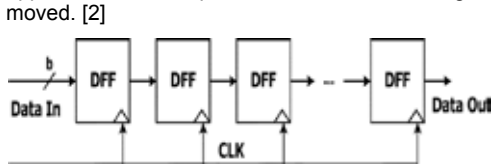

Fig.2: Delay buffer implementing shift registers

In the pointer based design, a ring counter with only one rotating active cell to point the words for write-in and read-out. The bottom row of DFF is initialized with only one “1” and all the other DFFs are kept at “0”. When a clock edge triggers the DFFs, this “1” signal is propagated forward. Consequently, the traditional binary address decoder can be replaced by this “unary-coded” ring counter. Compared to the shift register delay buffers, this approach propagates only one “1” in the ring counter instead of propagating - bit words.

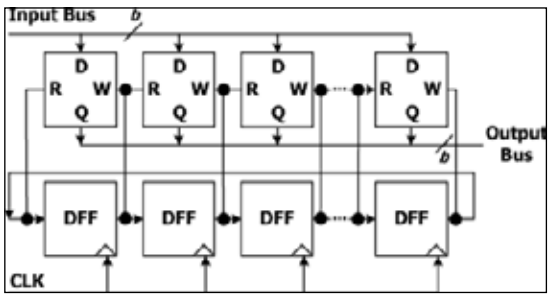

Fig.3: Pointer-based delay buffer

4. GATED CLOCK RING COUNTER

The ring counter which uses DET flip flop and C-elements are used for the generation of clock gating. To further reduce the activity along the clock distribution network, a gated clock driver tree is then applied. [2]

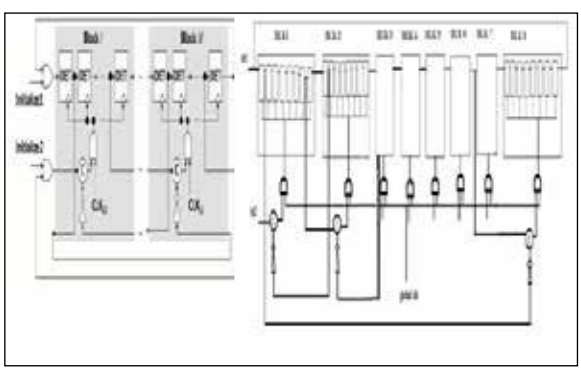

Fig.4: Ring counter with clock gated by C-elements

4.1 DET flip flop

Double edge triggered flip-fops are used to generate two outputs at a single clock pulse. In these flip-flops work will be done at rising edge and falling edge. Thus, clock frequency is reduced to one half.

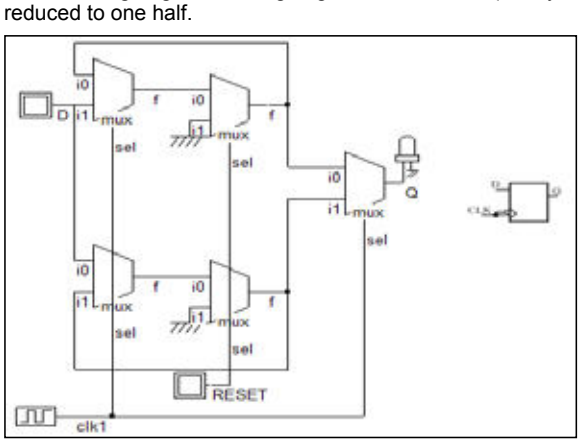

Fig.5: DET flip-flop

4.2 CLOCK GATING USING C-element

A gating function is used to turn off the clock to some of the functional module for some extended period of time.

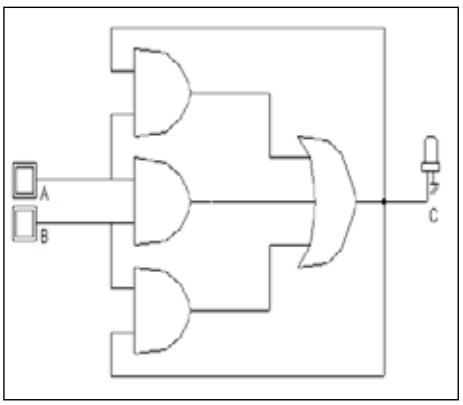

Fig.6: C-element

The logic express for C-element is given by

$C_{next} = AB + BC + CA$

where A and B are its inputs and C and C_{next} is the current and next output. If A=b, then the next output will be the same as the input. Otherwise, if A≠B, then output remains unchanged. Since the output of C-element can only be changed when A=B, it can avoid the possibility of glitches. It’s avoiding excessive clock loading. It’s works with hand shaking protocol.

4.3 GATED CLOCK DRIVER TREE

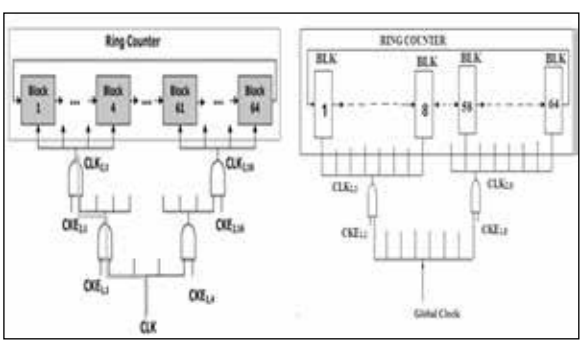

Fig.7: Tree structure clock tree drivers with gating in Quad and Oct system

Loading on the global clock signal “CLK” is diminished further by using this technique. This method efficiently reduces the length of clock path that distributed in whole circuit and distribution layers also get reduced by which the tree contains 8 leaf. A driver tree distribution network is used for the global clock and activated only those drivers along the path from the clock source to the blocks that need to be driven by the clock.

5. SRAM MEMORY

SRAM memory consists of latch, and gate and not gate. The circuit diagram is given below. When rw = ‘0’, data is store. When rw = ‘1’, data is read out.

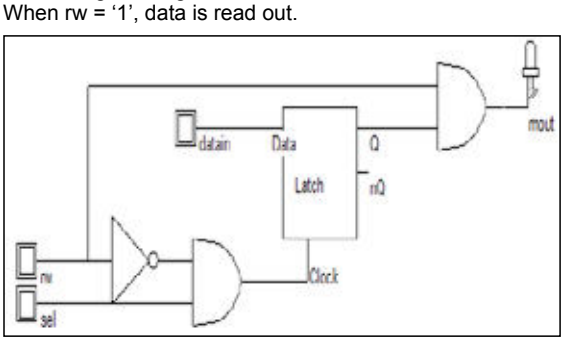

Fig.8: SRAM in both Quad and Oct system

6. GATED DRIVER TREE FOR INPUT AND OUTPUT

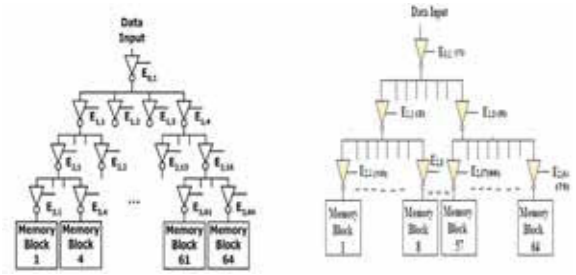

Fig.9: Gated driver tree of input driving circuitry in Quad and Oct system

This technique can eliminate the power wasted on the drivers that need not be activated. Of all the memory cells, only two words will be activated: one is written by the input data and the other is read to the output. Driving the input signal all the way to all memory cells seems to be a waste of power. The same is in the case of read circuitry of the output port. In the input driving/output driving sensing circuitry in the memory module of the delay buffer, the gated clock tree technique is used. For the input, or gate and tristate buffer is used while for output multiplexer and encoder are used.

7. RESULTS

Fig.10 shows the simulation for the Oct system delay buffer using ModelSim 6.6d for eight bits.

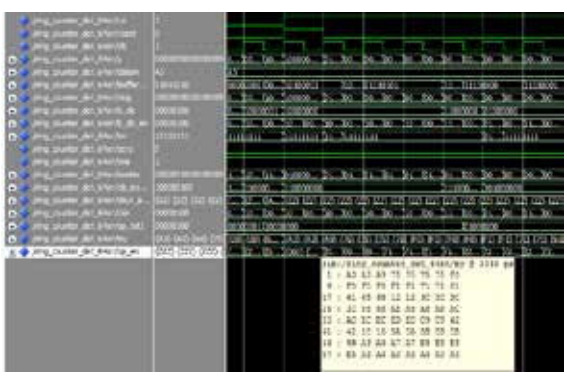

Fig.10: Simulation result for delay buffer

Fig.10 shows the formation of mask file for the Oct system delay buffer using Microwind 3.1 for one bit.

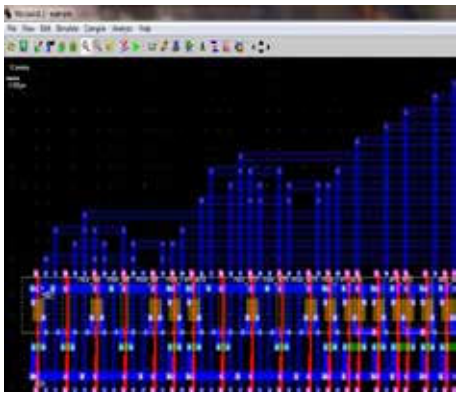

Fig.11: Forming the Mask file for
Backend by using Microwind 3.1

Table 1 show the simulated power for one bit of data in Microwind 3.1for backend part after creating mask file.

Table 1. Power analysis using Microwind 3.1(Time Scale 1ns)

Simulated Power @(2.5V, 1.2V), 568MHz,Time Scale 1ns , CMOS 90nm		
STRUCTURE	QUAD SYSTEM (mW)	OCT SYSTEM (mW)
Gated Ring Counter Structural 32 bits	0.635	0.458
Gated Ring Counter Structural 64 bits	1.160	0.781
Delay Buffer for 64bits	3.516	3.320

Table 2 show the power synthesis for eight bits of data in Altera Quartus II 10.0 in Cyclone II FPGA for frontend part after writing the VHDL coding.

Table 2. Power synthesis using Altera Quartus II 10.0 in Cyclone II FPGA

STRUCTURE	QUAD SYSTEM (mW)	OCT SYSTEM (mW)
CLOCK TREE	33.16	31.10
INPUT TREE	215.53	210.43
OUTPUT TREE	260.71	259.11
DELAY BUFFER	39.02	39.01
TOTAL	548.42	539.65
❖ DIFFERENCE = 8.77 mW		

8. CONCLUSION

Measurement results indicate that the Oct system consumes less power than the Quad system that measured both in Frontend tool and Backend tool.

9. FUTURE WORK

In future, considering the effective approach design for the memory section will result in more power saving.

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