Research Paper Engineering

Evolvable Hardware Filter for Surface Roughness

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ABSTRACT

In recent years machine vision has become a main stream to replace human vision in high speed manufacturing techniques. Image acquired through modern cameras are contaminated by a number of noise sources with decreasing intensity,the proposed architecture Evolvable hardware uses reconfigurable Xilinx Virtex2.The evolutionary enhanced image is processed and compared stylus method. This method of measuring the surface roughness is with low noise,faster and lower price.

Keywords : Evolvable hardware,Surface roughness,Image enhancement,FPGA.

I.INTRODUCTION

Images acquired by modern cameras are contaminated by a number of noise sources and also get distorted. Hence preprocessing unit is required to improve image quality. For effective processing of the image, requires computing architecture that is highly flexible, more cost-effective and less complicated. In this paper, the image processing is done using evolvable hardware (EHW) architecture and is implemented for high performance in noise filter. In this work, the evolved circuit has better performances and is optimized with different parameters. After grabbing the images using the EHW system, the quality images of surfaces used for surface finish. FPGA implementation of the circuit allows fast computation and complex, by dedicated hardware. As hardware units can be operated in parallel and also makes it ideally suited for online applications.

II. LITERATURE REVIEW

Competitive world has focused attention on manufacturers to increase improve quality and productivity. The surface quality of the machined parts plays a important role in the performance and significantly influences the corrosion resistance, creep life, fatigue strength, etc. Surface roughness also affects functionalities' such as friction, wear, heat transmission, ability of distributing, and light reflection, etc. In recent years, computer vision technology has gained tremendous vitality in all fields. As new applications grow and several investigations have been carried out on surface roughness of a work piece. Machine vision can grab the images online without accounting the factors like vibrations of machine tool, noise etc. [4] utilized statistical parameters, derived from grey level intensity histogram such as range and the mean value of distribution and correlated with the Ra value determined from the stylus method. Ramamurthy et al. [12,13] have utilized the grey level intensity histograms, etc. for new optical parameters for roughness evaluation. Carneiro [11] measured the surface roughness using scanning microscopy, which includes more than 20,3-D roughness parameters to characterize the surface topography. After capturing the images of surfaces using machine vision systems manufactured by various processes.

III. SYSTEM MODEL

A. EVOLVABLE HARDWARE

In evolvable hardware, how well the proposed design solve the particular task is done by fitness evaluation. A new design proposal can be started up when the current design fails to work satisfactory. If the evolution process is on chip, adaption does not need to decided at the design time, the required change in circuit is freely evolve dynamically with varying factors. The evolvable hardware is shown in the below Figure 1. The field of evolvable hardware is shown as the intersection of Computer Science, Electronic Engineering and Biology.

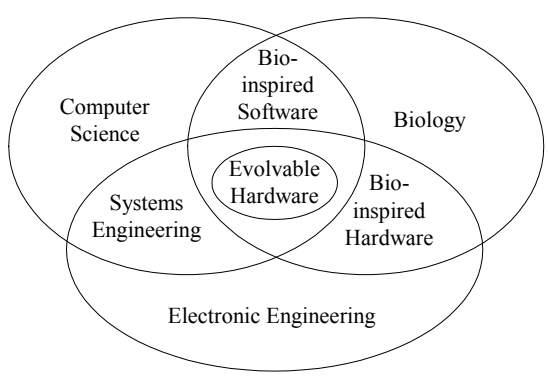


Figure.1 Evolvable hardware originates from the intersection of sciences.

The hardware design and synthesis, evolutionary computation are as shown below in figure 2. Digital hardware is traditionally a combination of processes. A designed circuit specification are mapped to a logical representation to the process of logic synthesis. The circuit design, along with optimisation decisions during the synthesis process is the domain of the human designer. It's significant interest has developed in implementing evolutionary techniques in the VLSI design flow at circuit design, this can allow to generate creative design. EHW is a hardware which is built on software reconfigurable logic devices such as PLD and FPGA and whose architecture can be reconfigured using genetic learning.

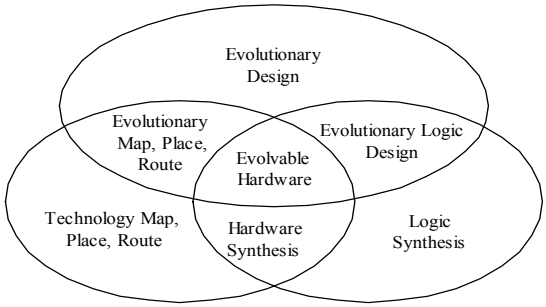


Fig.2 Evolvable hardware design and optimization techniques.

EHW which is built on software reconfigurable logic blocks such as PLD and FPGA,whose architecture can reconfigured using genetic learning. To design conventional hardware, it becomes necessary to prepare all the specifications of hardware functions in advance. EHW can be reconfigure without such specifications. The basic idea of EHW is a reconfigurable device as a chromosome for GA, which searches for an optimal hardware structure. The GA chromosome, that is the architecture bits, is downloaded onto the reconfigurable device during genetic learning.

B. MERITS OF EHW FILTER

General image filters lacks the adaptability for un-modeled noise types and flexibility. Evolutionary algorithms based filter architectures are capable to provide solutions to hard design problems. Using this approach, it is possible to have image filter that can employ a complete design by an evolutionary algorithm. An evolutionary algorithm filter is designed with the kernel or the whole circuit being automatically evolved. The EHW architecture proposed can evolve filters without priori information. This architecture considers spatial domain approach and use the overlapping window to filter the signal. This approach is chosen to find the best filter configuration.

C. IMAGE ENHANCEMENT USING EVOLUTIONARY DESIGN

The EHW architecture proposed is to filter the noise present in the image and subsequently realized on FPGA based image processing board consist of the genetic algorithm a virtual reconfigurable circuit and processor is shown in Figure 3 This implementation is a combination of hardware realization of genetic algorithm and a reconfigurable device. These two modules of the EHW are described in the below sections:

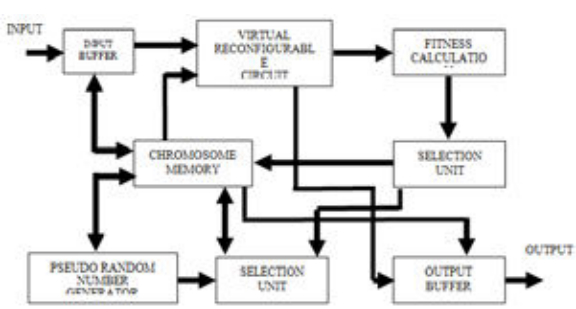


Figure 3 EHW chip with the GA Processor and VRC

D. IMPLEMENTION OF VRC

VRC is implemented as a combinational circuit using the concept of pipelining. This consists of processing elements in columns and rows. In this work, a total of 25 PE's are selected and arranged in four columns and six rows representing the final output.

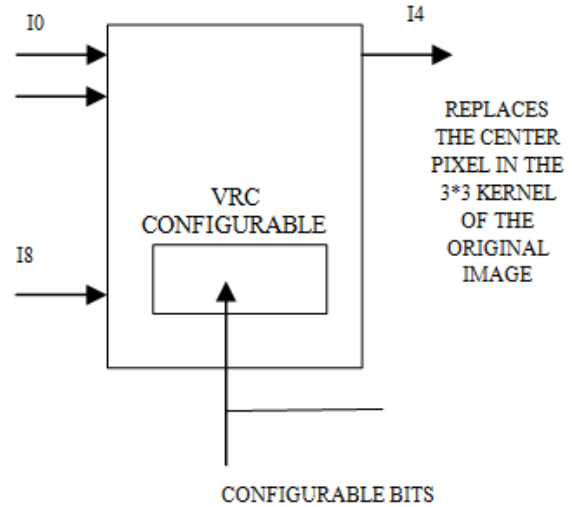


Figure 4 Architecture of VRC

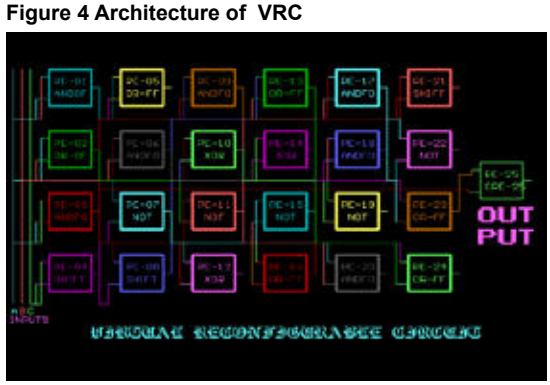


Figure 5 Virtual Reconfigurable Circuit

I_4 represent filtered output of the VRC. The operation performed on input, depends on the bits downloaded into configurable memory from the GA unit.

E. EVOLVING IMAGE OPERATORS FOR PREPROCESSING

The function performed by each PE is selected from a set of evolved operators so that the evolved circuit is testable without the need of data path. Total of 16 functions are selected and given in Table 1. Another feature of this work is using the primary inputs and outputs, the evolved circuit can be tested. It is assumed that none of the inputs of elements are connected to the same data source. From figure 6, Slice 1 'm' bit vector is selects any one of many inputs and assigns it first input X.Slice 2 'm' bit vector and selects any one of many inputs and assigns it as second input Y.

TABLE 1 EVOLVED IMAGE PROCESSING OPERATORS

Function Code	Function	Function Code	Function
0000	X >> 1	1000	X & 0x0F
0001	X	1001	X & 0xF0
0010	~ X	1010	X | 0x0F
0011	X & Y	1011	X | 0x F0
0100	X | Y	1100	Min (X,Y)
0101	X ^ Y	1101	Max (X,Y)
0110	(X+Y)>>2	1110	Y<<1
0111	(X+Y) >>1	1111	X+Y

Slice 3 is 'n' bit vector and selects any one of 16 functions to be performed on X and Y

The X and Y are both 8-bit vectors and processed output is also an 8- bit vector.

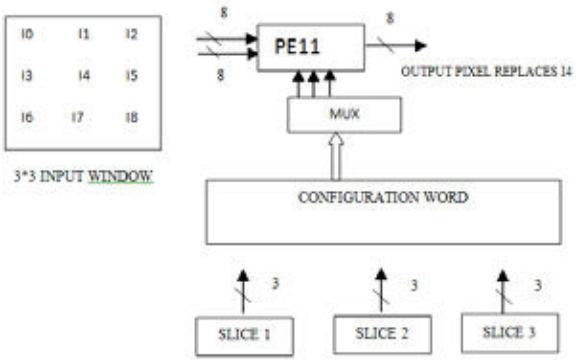
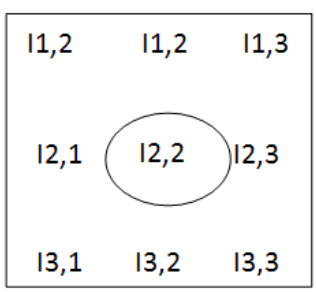


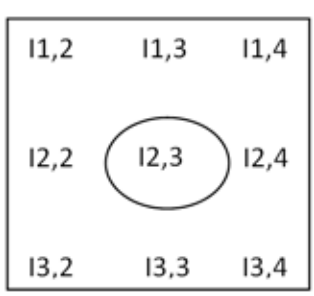
Figure 6.VRC with MUX for selecting inputs and functions

IV. FILTERING ALGORITHM FOR IMAGE NOISE.

The choice EHW architecture for image enhancement is described in this section. Using this architecture noise is removed from the image. Generate initial population of size 'n' with a chromosome length L. Each chromosome contains the details, of PE's interconnected and the function is performed by the PE. Assume 3x3 overlapping window, input the nine pixel value to the VRC which processes and replaces the center pixel. Every pixel value of a filtered image is processed using a corresponding pixel and its eight neighbors. This process is illustrated in Figure 6 and repeate for the whole image. Calculate the Mean Difference Per Pixel (MDPP) using the reference image and assign it as fitness value. Retain the chromosome that has maximum fitness.



.Stage I 1st 3x3 window presented to VRC and I2,2 replaced by filter output



Stage II 2nd 3x3 window presented to VRC and $I_{2,3}$ replaced by filter output

Figure 7. Different Pixel Windows processed by the evolved circuit

In Figure 7 $I_{p,q}$ represents the pixel value at p^{th} row and q^{th} column respectively. The window presented as inputs to the evolved circuit employs a spatial filtering approach.Apply the crossover and mutation operation on the selected chromosome to get the next generation strings. The roulette wheel selection procedure is chosen in this work. Replace the old population Repeat for a specified number of generations 'N'.

V.FPGA IMPLEMENTATION

To create an FPGA design, a designer have several options for algorithm implementation. VHDL is chosen as a target design language in the work because of familiarity and wide-ranging support, in terms of software tools and vendor support. In the first state, a design is created in VHDL,then the code's syntax is verified and the design is synthesized, compiled, into a library. The design is simulated to check its functionality. The design is processed and mapped onto a specific FPGA in software.

The VHDL code, algorithm described above is developed and imported into the Xilinx FPGA image processing board. The EHW is configured to nine 8-bit inputs I0 – I8 and produce a 8-bit output which processes gray-scaled images. Each pixel value of the filtered image is calculated by using a corresponding pixel and its eight neighbors as discussed. The operation on the selected input pixels depends on configuration bits downloaded into configurable memory from genetic unit. The VRC consists of 2 5 PEs as shown in Figure 6. Four PEs are implemented as a single stage of the pipeline.

Each PE processes two 8-bit inputs and produce single 8-bit output. The outputs of PEs equipped with registers. The two inputs of every PE can be connected to one of the outputs from the previous *l* columns where *l* is the level back parameter. In this work, *l* is chosen as '2'. Every PE executes a certain function from Table 1, depending on the function code configuration, sel3 which is applied to its two inputs.

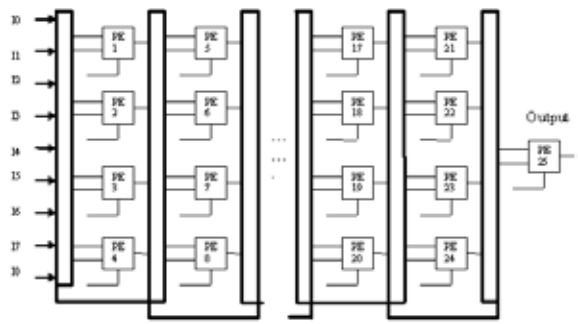


Figure 7 Architecture of the Virtual Reconfigurable Circuit

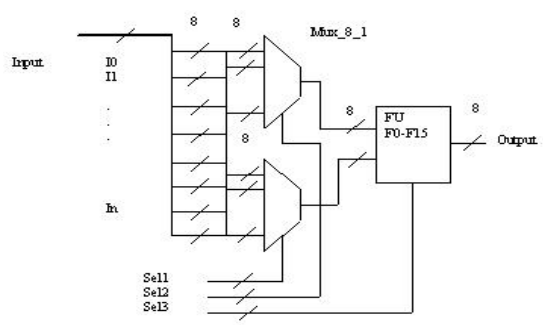


Figure 8. Architecture of a Single Processing Element

The architecture of single PE is shown in Figure 8. The configuration bit stream consists of ten bits for each PE. The output of the PE is given by

The fewer the functions, the faster is the evolution. Further functions can be included but this is dependant on the resource requirements, as there is a trade-off between the functionality and the complexity of the hardware structure.

VI.RESULTA AND DISCUSSION

The images grabbed using CCD camera are passed to EHW chip to remove the unwanted noise. After preprocessing the quality of image is improved.

A input image with resolution m*n the chip replaces the original low quality out image.The number of initial population is

set to be 16,each chromosome is evolved with crossover 0.9 where as mutation 0.01.The quality of the image increases by 80% EHW filter.

Figure.9 Raw Image

Figure.10 Evolvable hardware processed image.

The surface finished EHW values are compared with raw image and stylus technique,are listed below.

Table 2 Comparision of surface roughness in different techniques

S.No	Raw Image G_a	EHW G_a	R_a Stylus (µm)	R_a Raw Image (µm)	R_a EHW (µm)
1	29.07	23.28	4.43	4.90	4.60
2	59.40	34.00	12.74	9.21	13.65
3	88.93	61.27	32.50	26.58	27.72
4	25.04	19.89	3.20	2.54	3.05
5	58.17	44.53	9.87	10.62	10.12
6	52.32	34.86	10.22	9.32	9.62
7	21.06	23.48	1.61	1.93	1.83

VII.CONCLUSION

A novel EHW based image filter is used to remove the noise present in the image is designed and implemented on Xilinx FPGA based image processing board. A reconfigurable architecture image enhancement enables the addition of new image features, allows rapid implementation of new standards and protocols on an as-needed basis and protects the investment in computing hardware. It functions as a programmable hardware with higher performance, flexibility of a software based solution while retaining the execution speed of a more traditional hardware based approach.

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