Volume : 2 | Issue : 9 | Sept 2013 ISSN - 2250-1991

Research Paper Engineering

A Novel Approach of Repair in Bisr For Ram's

* T. Dedeepya ** P. Kalpana Reddy

* Master of Technology (ECE) & H.NO:2-3-137, Road No-17, Co-operative bank colony, Nagole, Hyderabad,Andhra Pradesh. PIN- 500068

** Associate Professor and Head of the Department, Progressive Engineering College

ABSTRACT

Built-in self-test (BIST) refers to those testing techniques where ancillary hardware is added to a design so that testing is proficient without the aid of exterior hardware. Generally, a pseudo-random producer is used to apply experiment vectors to the circuit under experiment and a data compactor is used to build a signature. To raise the consistency and yield of embedded reminiscences, numerous redundancy mechanisms have been planned. The entire redundancy mechanisms bring corollary of area and complexity to embedded reminiscences design. Considered that compiler is used to organize SRAM for different needs, the BISR had better bring no change to other modules in SRAM. To solve the problem, a new redundancy scheme is proposed in this paper. Some normal words in embedded reminiscences can be selected as redundancy instead of adding spare words, spare rows, spare columns or spare blocks. Built-In Self-Repair (BISR) with Redundancy is an effective yield-enhancement strategy for embedded reminiscences. This paper proposes a professional BISR strategy which consists of a Built-In Self-Test (BIST) module, a Built-In Address-Analysis (BIAA) module and a Multiplexer (MUX) module. The BISR is designed bendable that it can afford four operation modes to SRAM users. Each fault address can be saved just once is the feature of the proposed BISR strategy. In BIAA module, fault addresses and surplus ones form a one-to-one mapping to achieve a high repair speed. Besides, instead of adding spare words, rows, columns or blocks in the SRAMs, users can select typical words as redundancy. Now a day's we are using the new memory technologies. These technologies involving high density of shrinking devices lead to newer faults. These new faults cannot be simply detected by established experiments like March C, depiction it insufficient/ inadequate for today's and the future high speed reminiscences. More appropriate test algorithms are required. March SS algorithm is a newly developed test algorithms that deal with detecting some newly developed newer faults.

Keywords : BISR, Built-In Self-Test, Faulty address.

INTRODUCTION:

Today's deep submicron technologies allow the execution of multiple reminiscences on a single chip. Due to their high density, reminiscences are more prone to faults. These faults impact the total chip yield. One way to solve this problem is to augment the memory by surplus memory locations. The address mapping of the fault free working memory is programmable within certain limits. In order to do so, a memory experiment is needed to identify the faulty regions. The memory is tested by external test hardware or by on chip dedicated hardware (memory BIST). The second testing strategy is the preferred method for embedded reminiscences. After memory testing the memory address map is programmed by means of volatile or non-volatile storage on or off chip. To provide the analysis pattern from a memory BIST a multiplexer in front of the memory is widely used. The redundant spare rows and spare columns are often included into the memory. This impacts the performance and area conditions of the memory. The memory is repaired during testing by storing faulty addresses in registers. These addresses can be streamed out after test completion. Furthermore, the application can be started immediately after the memory BIST passes. The redundancy logic calculation will not increase the test time of the memory BIST.

BISR IMPLEMENTATION:

BISR: Combining BIST with efficient and low cost repair schemes in order to improve the yield and system reliability as well. March SS [5] and March RAW [3] are examples of two such newly developed test algorithms that deal with detecting some newly developed static and dynamic fault models. New microcode BIST architecture is presented here which is proficient of employing these new test algorithms. A word-oriented BISR array is used to repair the faulty memory locations as indicated by the BIST controller. The interface of repair array with BIST controller and Memory under test is shown in Fig.1

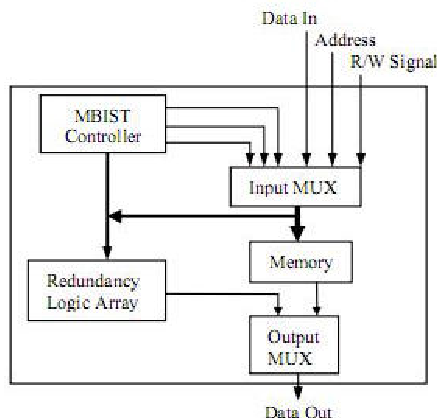


Fig.1 Block Diagram of BISR

 ISSN - 2250-1991

ARCHITECTURE OF BISR:

The architecture of BISR which have been developed to execute prior tests like March C may not be able to simply execute these newer test algorithms. The reason is that most of the newly developed algorithms have up to six or seven (or even more) number of test operations per test part. For example test parts M1 through M4 of March SS algorithm have five test operations per part. This is in contrast with some of the algorithms developed prior like March B, MATS+, March C which only had up to two operations per March part. Thus some of the newly developed architectures [6] older algorithms can only execute up to two march operations per march part, depiction them in proficient of simply executing the new test algorithms. March algorithms profitably executed and applied using this architecture. This has been illustrated in the present work by executeing March SS algorithm. The same hardware has also been used to execute other new March algorithms. This requires just changing the Order storage unit, or the order codes and sequence inside the order storage unit. The order storage unit is used to store predetermined test pattern. The architecture of the micro based built in self test and repair is shown In the Fig.2.

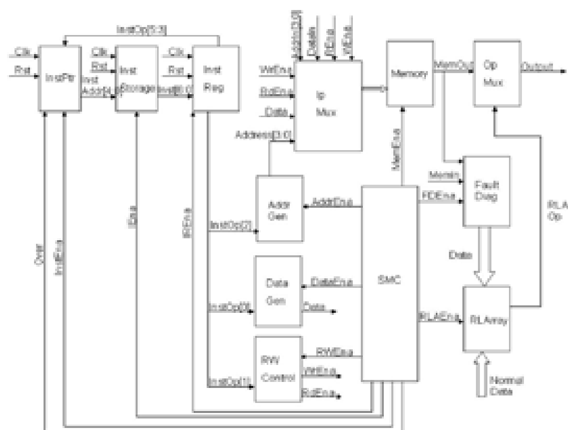


Fig.2 Architecture of Built in Self Test and Repair

The block diagram of the BIST controller architecture together with fault diagnosis interface through input MUX shown in above Fig.2.

March tests: This section introduces a new march test, March SS, after which a comparison with current industrial march tests will be made. However, first the March notation will be given.

March Notations: A complete march test is enclosed by the '{:::}' bracket pair, while a march part is enclosed by the '(:::)' bracket pair. March parts are separated by semicolons, and the operations within a March part are separated by commas. Note that all operations of a March part are performed at a certain address, before proceeding to the next address. The latter can be done in either one of two address orders: an increasing or a decreasing address order. When the address order is not relevant, the symbol is used.

March SS: March SS is shown in Figure 3. It has a test length of 22n, and detects all single-cell and two-cell presented in Section 3. Minimization of the test length of the test was considered a high priority. However, M5 can be extended (e.g., (r0; r0; w0; r0; w1)) if a regular structure is required for BIST applications. Let Mi,j denote the jth operation of march part Mi; e.g., M1,3 denotes the third operation (i.e., w0) of M1.

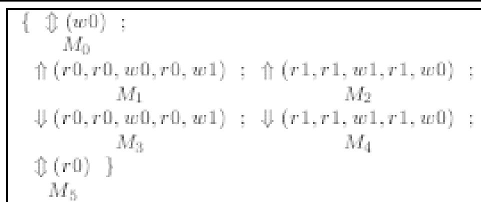


Fig.3 March SS

PROPOSED SYSTEM:

This paper proposes a professional BISR strategy which consists of a Built-In Self-Test (BIST) module, a Built-In Address-Analysis (BIAA) module and a Multiplexer (MUX) module. The BISR is designed bendable that it can afford four operation modes to SRAM users. Each fault address can be saved just once is the feature of the proposed BISR strategy. In BIAA module, fault addresses and surplus ones form a one-to-one mapping to achieve a high repair speed. Besides, instead of adding spare words, rows, columns or blocks in the SRAMs, users can select typical words as redundancy. Now a day's we are using the new memory technologies. These technologies involving high density of shrinking devices lead to newer faults. These new faults cannot be simply detected by established experiments like March C, depiction it insufficient/ inadequate for today's and the future high speed reminiscences. More appropriate test algorithms are required. March SS algorithm is a newly developed test algorithms that deal with detecting some newly developed newer faults.

WORD REDUNDANCY BISR: The BISR mechanism used here employs an array of redundant words placed in parallel with the memory. These redundant words are used in place of faulty words in memory. For active interfacing with already existing BIST solutions as shown in Fig.1, the following interface signals are taken from the MBIST logic:

1) A fault pulse indicating a faulty location address
2) Fault address
3) Expected data or correct data that is compared with the results of Memory under test.

The MBISR logic used here can function in two modes.

A. Mode 1: Test & Repair Mode, in this mode the input multiplexer connects test collar input for memory under test as generated by the BIST controller circuitry. As faulty memory locations are detected by the fault diagnosis module of BIST Controller, the redundancy array is programmed. A redundancy word is as shown in Fig 4.

The fault pulse acts as an activation signal for program the array. The redundancy word is divided into three fields. The FA (fault asserted) indicates that a fault has been detected. The address field of a word contains the faulty address, here as the data field is programmed to contain the correct data which is compared with the memory output.

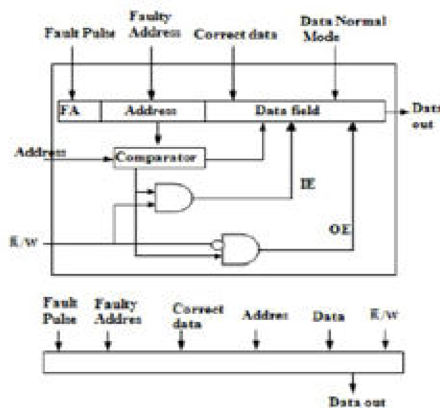
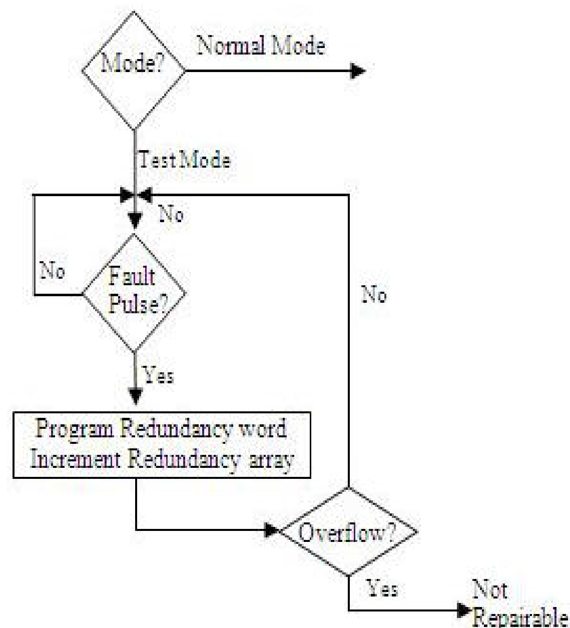


Fig.4: Redundancy Word Line

The IE and OE signals respectively act as control signals for writing into and reading from the data field of the redundant word. An overflow signal indicates that memory can no longer be repaired if all the redundancy words have been programmed. The complete logic of program of memory array is shown in Fig.5 below.

B) Mode2: Normal, during the normal mode each incoming address is compared with the address field of programmed redundant words. If there is a match, the data field of the redundant word is used along with the faulty memory location for reading and writing data. The output multiplexer of surplus Array Logic then ensures that in case of a match, the redundant word data field is selected over the data read out (= 0) of the faulty location in case of a read signal. This can be simply understood by the redundancy word.



Below Fig. 6, shows the repair module including the redundancy array and output multiplexer and its interfacing with the existing BIST module.

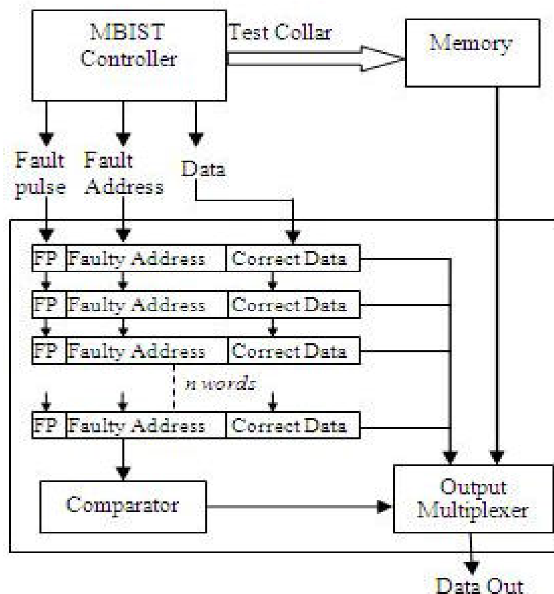


Fig.6: Repair module

CONCLUSION:

In this paper we have presented a new redundancy scheme with Built-In Self-Repair (BISR) which yields an effective enhancement strategy for embedded reminiscences. In this we have integrated a Built-In Self-Repair (BISR) strategy with a Built-In Self-Test (BIST) module and a new memory technology say March C by proposing March SS algorithm so, that it can afford two operation modes and algorithm results to SRAM users in order to improve the word redundancy. The BISR architecture is presented in this paper along with a March SS algorithm. Thus the word redundancy scheme is presented in this paper.

REFERENCES

[1]Said Hamdioui1, Ad J. van de Goor, Mike Rodgers(2002) "March SS: A Test for All Static Simple RAM Faults", International Workshop on Memory Technology, Design and Testing. | [2]D.S. Suk and S.M. Reddy, "A March Test for Functional Faults in Semiconductors Random-Access Memories", IEEE Trans. on Computers,. | [3] C-30(12), pp. 982-985, 1981. | [4] A.J. van de Goor, "Using March tests to test". | [5] Ravinder, N.Uma Rani," Design and Implementation of Built-in-Self Test and Repair", International Journal of Engineering Research and Applications, Vol. 1, Issue 3, pp.778-785. |